Drigmorn4 User Manual

Issue – 2.0

Kit Contents

You should receive the following items with your Drigmorn4 development kit:

1 - Drigmorn4 Board
2 - Programming Cable

Foreword

PLEASE READ THIS ENTIRE MANUAL BEFORE PLUGGING IN OR POWERING UP YOUR DRIGMORN4 BOARD.
PLEASE TAKE SPECIAL NOTE OF THE WARNINGS WITHIN THIS MANUAL.

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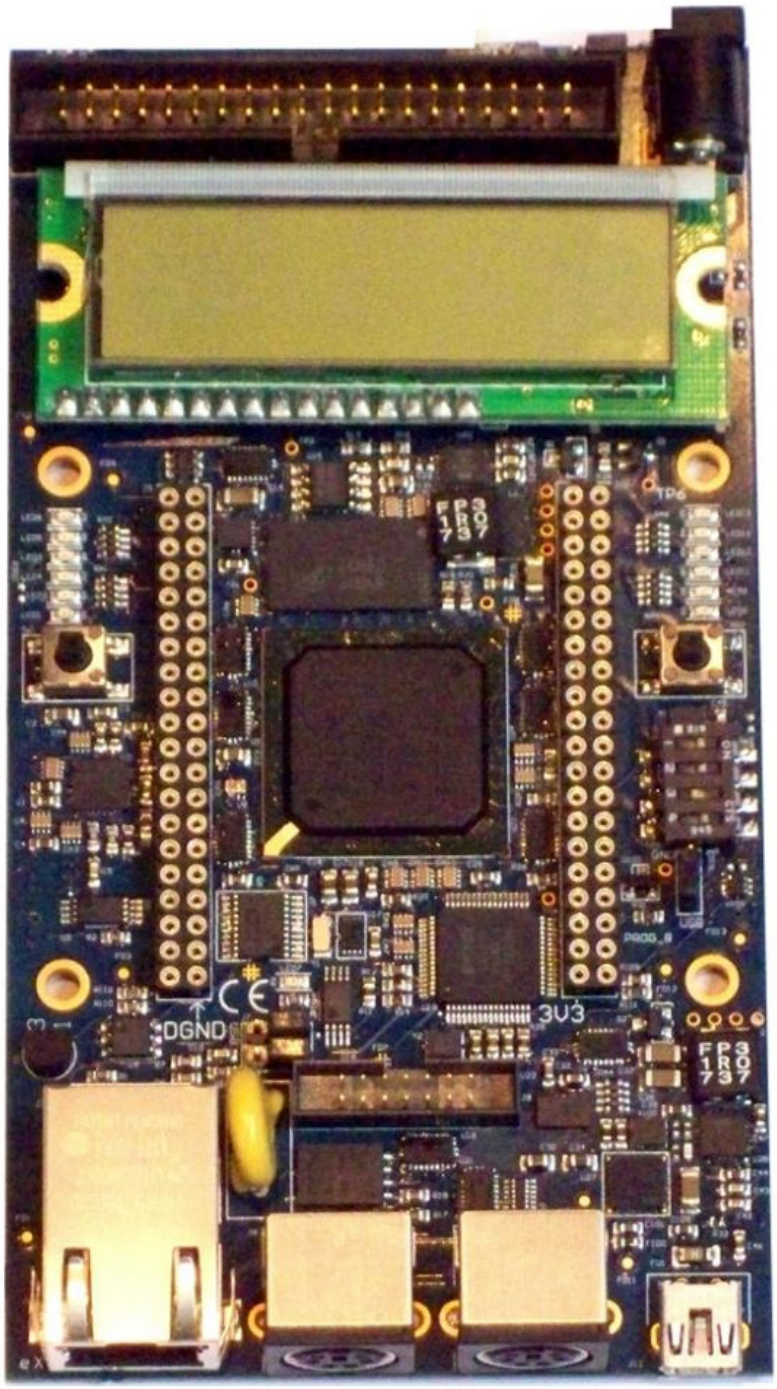
Drigmorn 4



Introduction

Welcome to your Drigmorn4 board. Drigmorn4 is a Spartan-6 based FPGA development board offering a highly powerful, flexible and low cost approach to prototyping FPGA and System designs.

The aim of this manual is to assist in using the main features of Drigmorn4. There are features that are beyond the scope of the manual. Should you need to use these features then please email support@enterpoint.co.uk for detailed instructions.

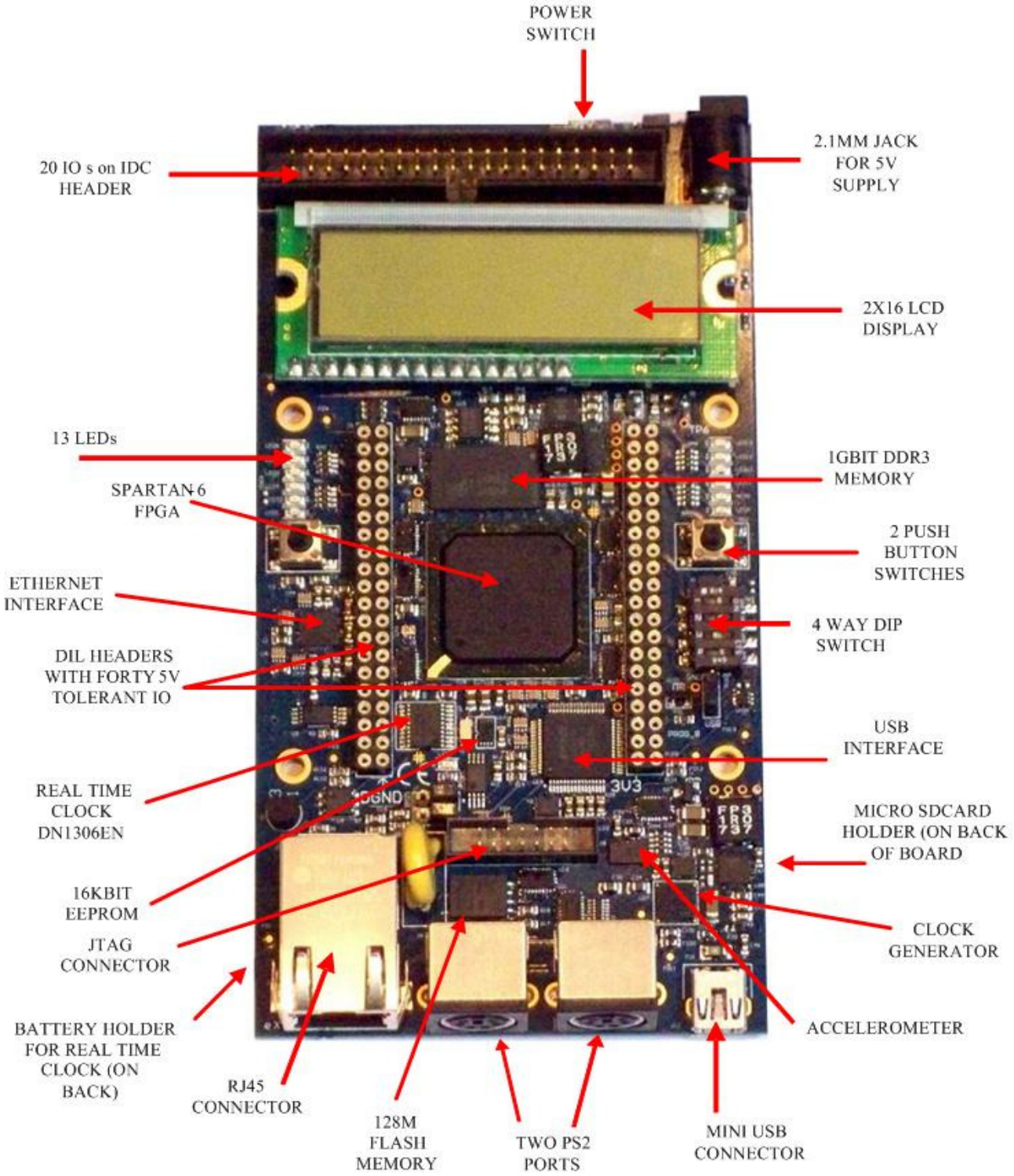
Drigmorn4 currently comes with a XC6SLX150-2FGG484C or XC6SLX75-2FGG484C Spartan-6. Other variants may be offered at a later date or as an OEM product. Please contact out us on boardsales@enterpoint.co.uk should you need further information.

Drigmorn4 is supported by a wide range of add-on modules. Some examples of these include:

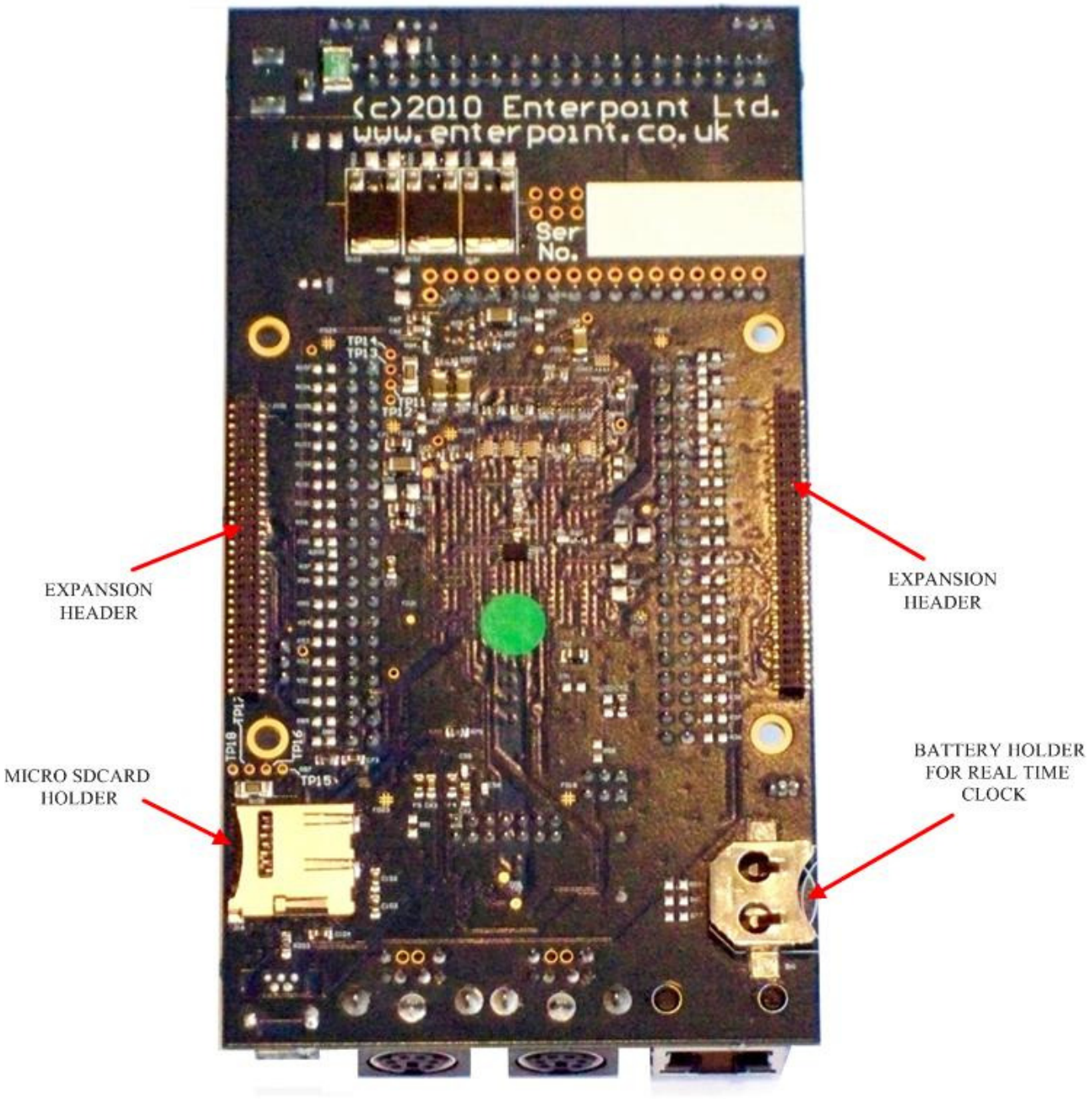
ADC 7927 MODULE
LED DOT MATRIX MODULE
BUTTONS/SWITCHES/SATA/MEMORY MODULE
RS232 AND RS485 HEADER MODULES
DP83816 ETHERNET MODULE
SD CARD MODULE
DDR2 MODULE
IDE/5V TOLERANT CPLD MODULE
USB MODULE
D/A CONVERTER MODULE
ADV70202 MODULE

We can also offer custom DIL Header modules should you require a function not covered by our current range of modules. Typical turn around for this service is 6-8 weeks depending upon quantity ordered and availability of components.

Getting Started



Drigmorn4 front View



Drigmorn4 Back View

Your Drigmorn4 will be supplied un-programmed. Unless you have bought an OEM product your board will be supplied with either a Prog2 parallel port programming cable or a Prog3 USB port programming cable.

The Xilinx toolset required to program the Drigmorn4 depends upon the Spartan6 device fitted to the board. If your Drigmorn4 is fitted with an LX75 device or smaller it is supported by the free ISE Webpack 11.1 SP4, or later, available from Xilinx providing all the tools to enter and build a design. Using this tool in conjunction with

your supplied programming cable you will also be able to program the Spartan-6, and the supporting SPI Flash, that are on Drigmorn4.

If your Drigmorn4 is fitted with an LX100 or LX150 device it will require the full Xilinx toolset to build a design.

ISE Webpack can be obtained directly from the Xilinx website at http://www.xilinx.com/ise. Registration will be necessary to complete the download. The full ISE toolset can also be purchased from the Xilinx website.

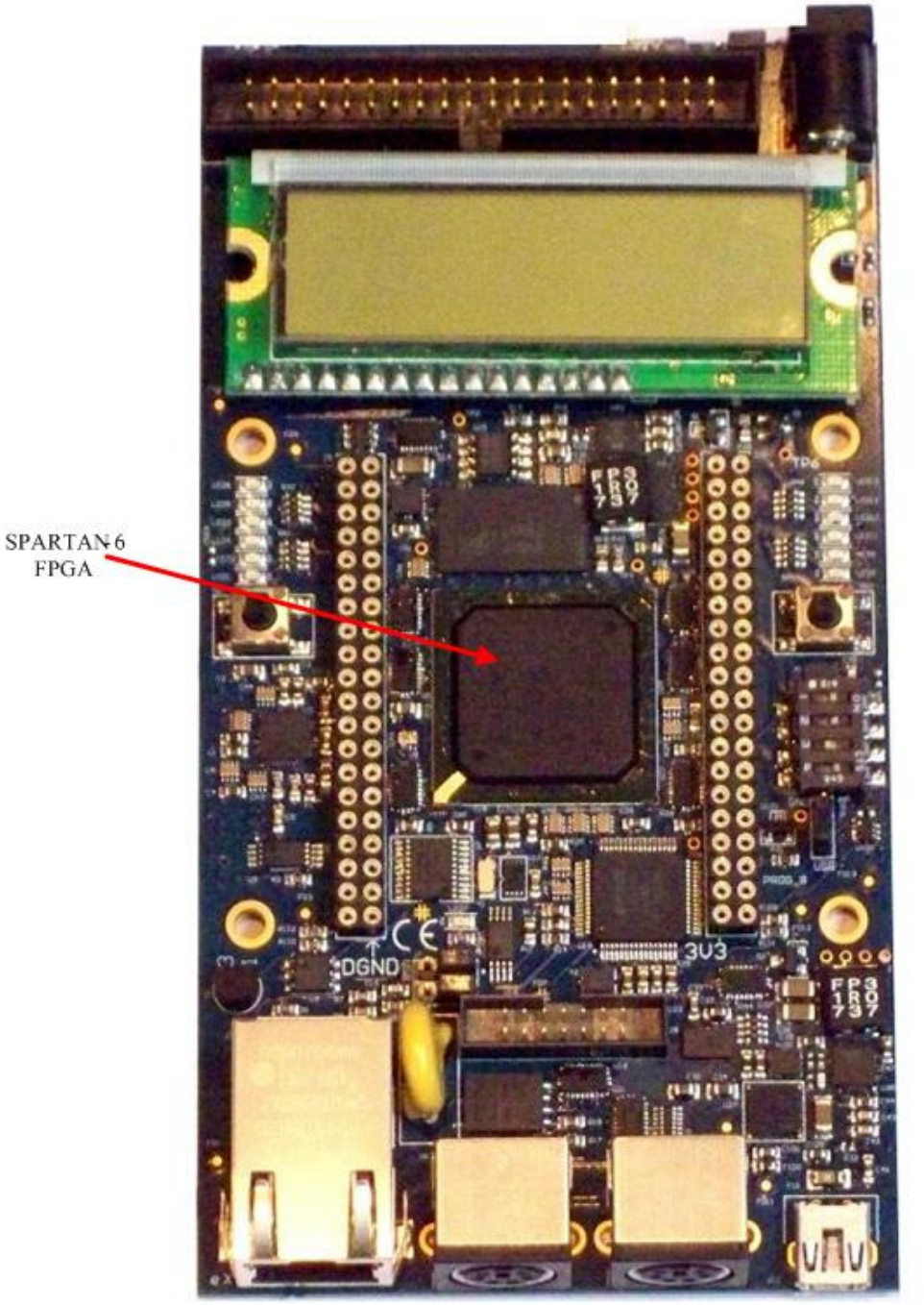
Once you have obtained your ISE tools:

(1) Connect your programming cable to the board and your PC hosting the Xilinx software.

(2) Connect the Drigmorn4 board to either a USB connector of a PC, a USB power supply or a 5V source plugged into the 2.1mm Jack socket. Note that some Laptops and desktop computer USB ports have a current limit of 100mA. Drigmorn4 can exceed this in some circumstances and should you have a problem a powered USB hub or external mains to USB adaptor are recommended solutions. Check that the 5V input selection jumper on J11 (situated adjacent to the 5V jack socket) is set to the correct position – left for power from USB, right for power into Jack socket. Switch the power ON using the small standby switch near J11.

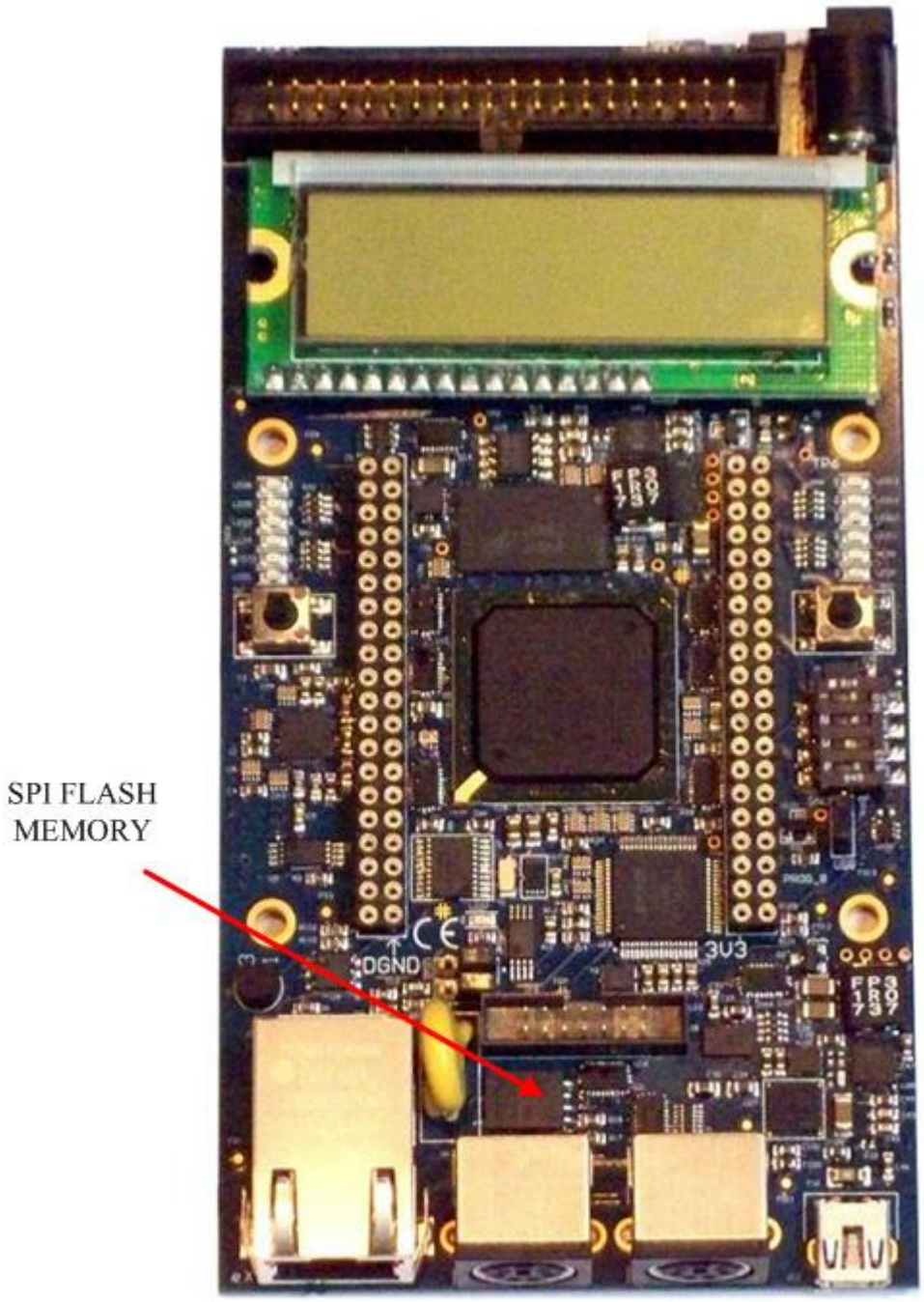
(3) If using an external power brick switch on your power source.

FPGA



Drigmorn4 supports Spartan-6 devices in the FGG484 package. Drigmorn4 is normally available with commercial grade -2 speed devices fitted in the XC6SLX150 or XC6SLX75 size. Should you have an application that needs industrial parts or faster speed grades please contact sales for a quote at boardsales@enterpoint.co.uk.

SPI FLASH MEMORY



The M25P128 SPI flash memory device configures the FPGA when it is powered providing a suitable bitstream is programmed into the device. The M25P128 has a capacity of 128Mbits with a single configuration bitstream for Drigmorn4 taking 4.1Mbits (LX150). Any remaining space can be used for alternative configurations or code and data storage.

After configuration the SPI Flash can be accessed via the following pins of the FPGA:

M25P128 FUNCTION	FPGA PIN
CCLK	Y21
MOSI	AB20
WRITE	V15
DIN	AA20
CSO_B	T5

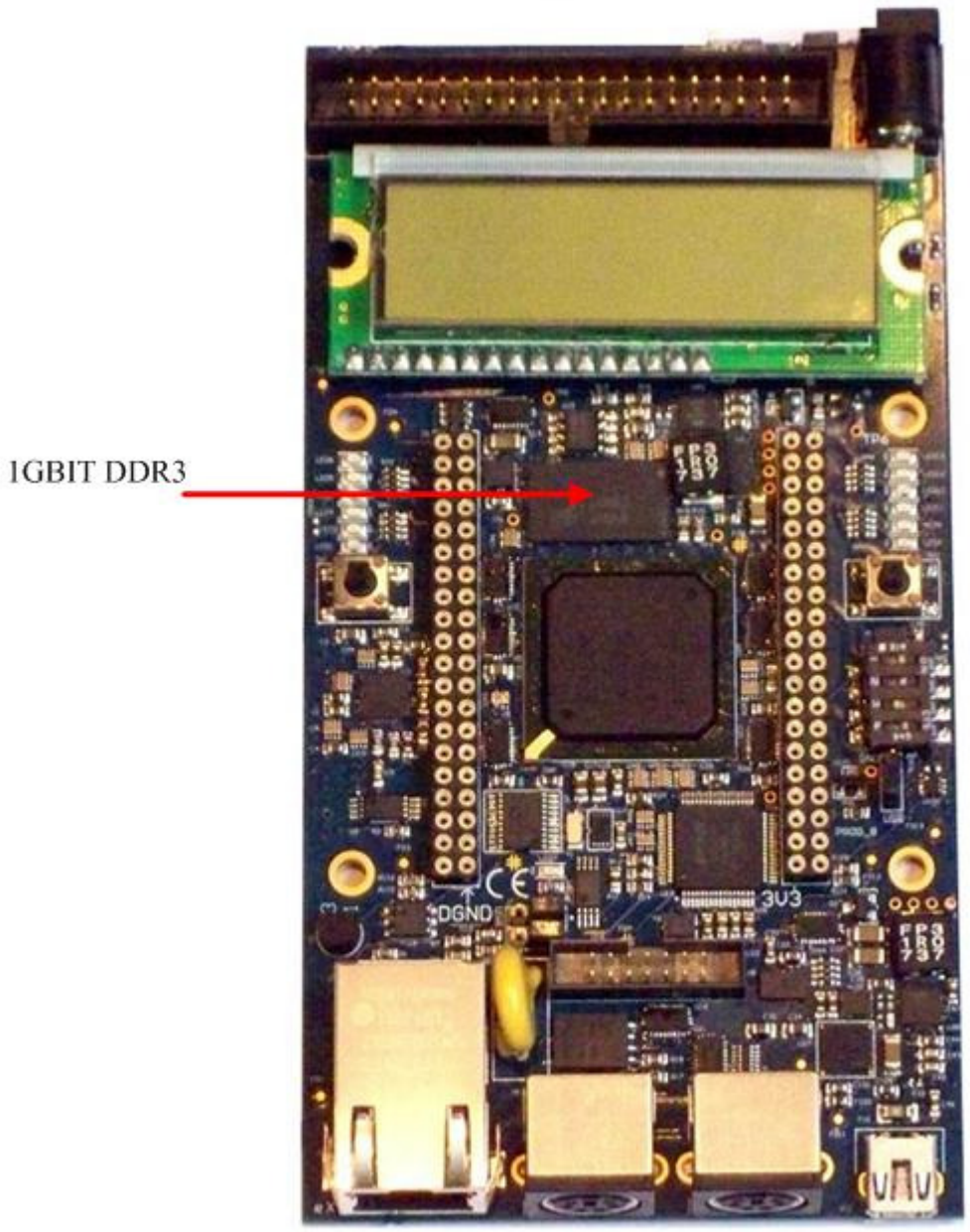
The HOLD pin of this memory device is permanently connected to 3.3V.

The flash memory can be programmed using direct SPI programming from the 7x2 programming connector J8. To achieve this the jumper J14 must be connected between pins 1 and 2 (left position). Otherwise the jumper J14 should be connected between pins 2 and 3 (right position) so that normal JTAG programming can be achieved.

The connections to the SPI flash can also be accessed via the USB interface. This option requires the jumper J14 to be connected between pins 2 and 3 (left position). The connections between the USB interface and the SPI flash memory are shown below:

M25P128 FUNCTION	USB SIGNAL NAME	FT2232 PIN
CCLK	BDBUS0	38
MOSI	BDBUS1	39
DIN	BDBUS2	40
CSO_B	BDBUS3	41

DDR3 MEMORY



Drigmorn4 has a 1GBIT DDR3 Micron MT41J64M16LA device as standard. This device is organised as 8 Meg x 16 x 8 banks. This device is supported by the hard core memory controller that is in the Spartan-6 FPGA. To add this core to your design the COREGEN tool, part of the ISE suite, will generate implementation templates in VHDL or Verilog for the configuration that you want to use. More details on the memory controller can be found in the user guide http://www.xilinx.com/support/documentation/user_guides/ug388.pdf.

The DDR3 has 12 address lines and 16 data lines to address all the available memory, which can be accessed at speeds of 1.87ns. More details of the DDR3 can be found in http://download.micron.com/pdf/datasheets/dram/ddr3/1Gb_DDR3_SDRAM.pdf.

For OEM applications we can fit bigger DDR3 parts subject to limitations of the memory controller.

The DDR3 site has the following connections to the FPGA:

DDR3 FUNCTION	FPGA PIN	DDR3 FUNCTION	FPGA PIN
DDR_A0	F21	DDR_DQ3	M22
DDR_A1	F22	DDR_DQ4	J20
DDR_A2	E22	DDR_DQ5	J22
DDR_A3	G20	DDR_DQ6	K21
DDR_A4	F20	DDR_DQ7	K22
DDR_A5	K20	DDR_DQ8	P21
DDR_A6	K19	DDR_DQ9	P22
DDR_A7	E20	DDR_DQ10	R20
DDR_A8	C20	DDR_DQ11	R22
DDR_A9	C22	DDR_DQ12	U20
DDR_A10	G19	DDR_DQ13	U22
DDR_A11	F19	DDR_DQ14	V21
DDR_A12	D22	DDR_DQ15	V22
DDR_A13	D19	DDR_LDM	L19
DDR_A14	D20	DDR_LDQS	L20
DDR_A15	B21	DDR_LDQS_N	L22
DDR_BA0	J17	DDR_UDM	M20
DDR_BA1	K17	DDR_UDQS	T21
DDR_BA2	H18	DDR_UDQS_N	T22
DDR_CS_N	P20	DDR_ODT	G22
DDR_RAS_N	H2	DDR_CAS_N	H22
DDR_WE_N	H19	DDR_RESET_N	F18
DDR_DQ0	N20	DDR_CKE	D21
DDR_DQ1	N22	DDR_CLK_N	J19
DDR_DQ2	M21	DDR_CLK	H20

The signals shown shaded in yellow are terminated using suitable arrangements of resistors.

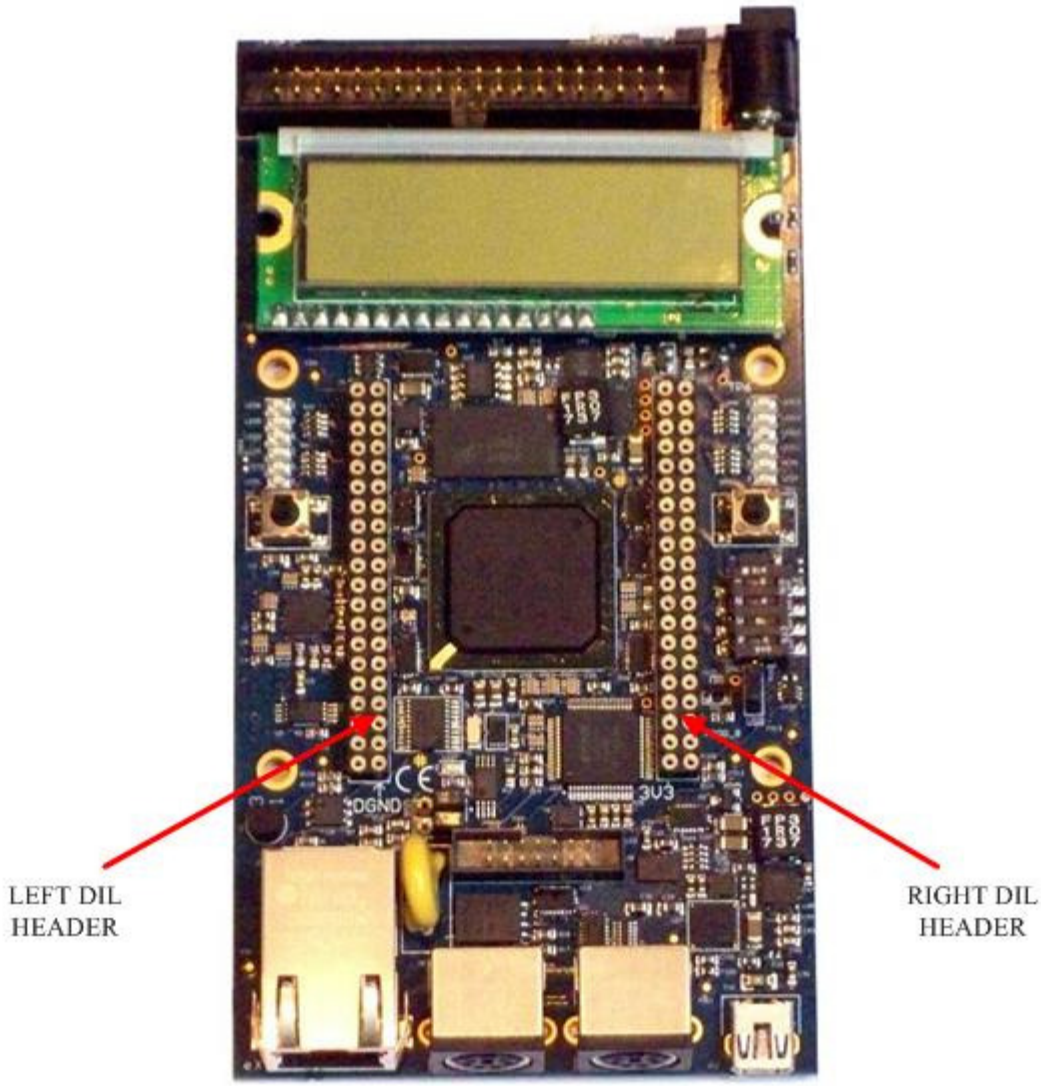
A timing loop has been implemented on the PCB and connected to the FPGA between pins **R19** and **P18** to facilitate compensation for temperature and timing delays where necessary.

DIL HEADERS

	LEFT COLUMNS				RIGHT COLUMNS		
	OUTER PINS		INNER PINS		INNER PINS	OUTER PINS	
ROW	FUNCTION	S6 PIN				FUNCTION	S6 PIN
1	IO_L65P_0	B18	0V		3.3V	IO_L2P_0	AA21
2	IO_L65N_0	A18	0V		3.3V	IO_L2N_0	AB21
3	IO_L63P_0	B16	0V		3.3V	IO_L5P_0	Y19
4	IO_L63N_0	A16	0V		3.3V	IO_L5N_0	AB19
5	IO_L50P_0	B14	0V		3.3V	IO_L14P_0	AA18
6	IO_L50N_0	A14	0V		3.3V	IO_L14N_0	AB18
7	IO_L37P_0	B12	0V		3.3V	IO_L15P_0	Y17
8	IO_L37N_0	A12	0V		3.3V	IO_L15N_0	AB17
9	IO_L35N_0	A11	0V		3.3V	IO_L19P_0	AA16
10	IO_L35P_0	C11	0V		3.3V	IO_L19N_0	AB16
11	IO_L34P_0	B10	0V		3.3V	IO_L31P_0	AA12
12	IO_L34N_0	A10	0V		3.3V	IO_L31N_0	AB12
13	IO_L6P_0	B8	0V		3.3V	IO_L45P_0	AA8
14	IO_L6N_0	A8	0V		3.3V	IO_L45N_0	AB8
15	IO_L4P_3	B6	0V		3.3V	IO_L49P_0	AB6
16	IO_L4N_3	A6	0V		3.3V	IO_L49N_0	AA6
17	IO_L5P_3	C7	0V		3.3V	IO_L57P_0	AA4
18	IO_L5N_3	A7	0V		3.3V	IO_L57N_0	AB4
19	IO_L32P_3	D7	0V		3.3V	IO_L64P_0	AA2
20	IO_L32N_3	D8	0V		3.3V	IO_L64N_0	AB2

The DIL Headers provide a simple mechanical and electrical interface for add-on modules. There are twenty I/O on each side of the DIL Header giving a total of 40 I/O available. Each of these I/O pins is protected by bus switch technology to facilitate 5V tolerance on all of these pins. Bus switch technology has a minimal effect on I/O timing with propagation times of less than 250ps through these devices. There are sites on the reverse side of the Drigmorn4 where pull-up resistors (to 5v) may be fitted. Drigmorn4 is normally shipped with these resistors not fitted. If customers require any of these resistors to be fitted it is advised that they specify which are required so that they can be fitted before the board is shipped. Enterpoint Ltd cannot be responsible for damage to the Drigmorn4 board by poor soldering.

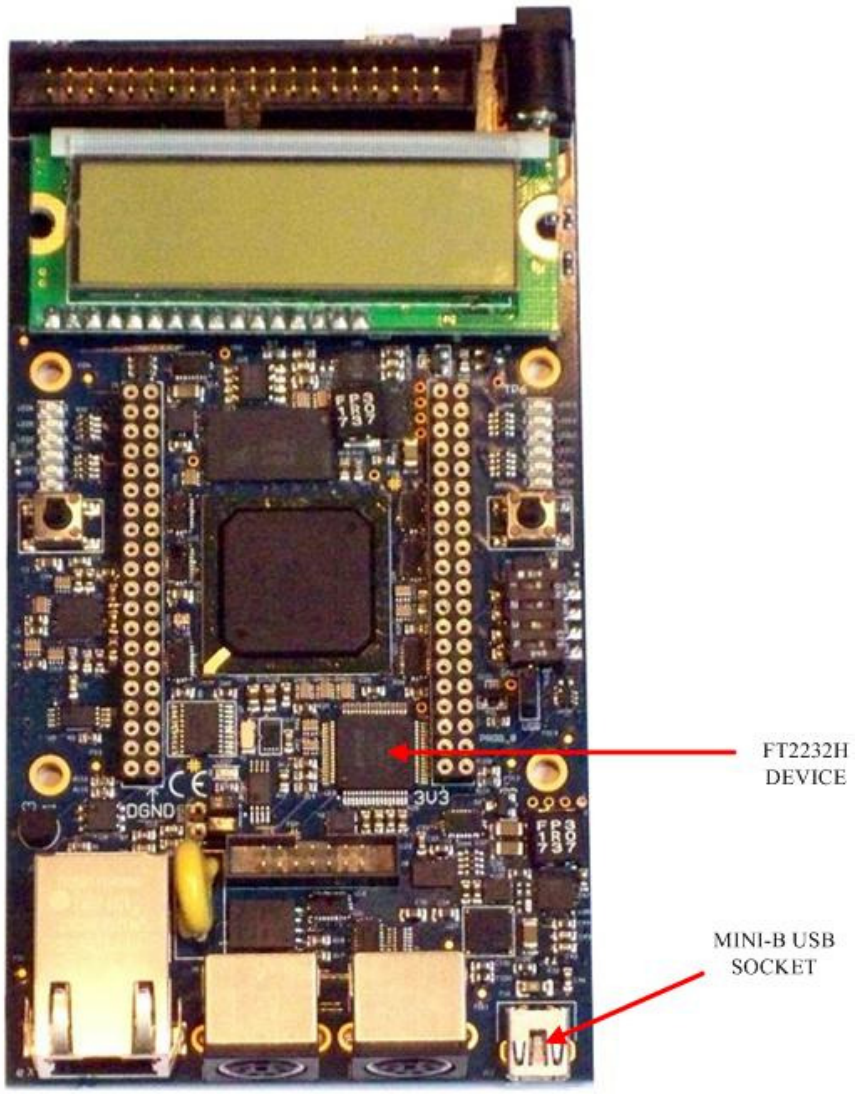
The DIL Headers can also support up 20 pairs of LVDS signalling when not used for add-on modules. The Spartan-6 FPGA can terminate any of these pairs. LVDS termination on individual signal pairs is a programmable option that can be set in build constraints for the FPGA when using the ISE toolset. The LVDS pairs are shown in the table above along with Spartan-6 pin numbers.



The DIL Headers support the use of add-on modules enhancing the capabilities of your Drigmorn4 board. Enterpoint has a wide range of modules suitable for the DIL Header. Details at http://www.enterpoint.co.uk/moelbryn/modules/modules.html. We can also offer custom design modules should our standard range not cover your requirement. The DIL Headers will also support the use of crude prototype circuits using stripboard or other prototype materials.

The DIL Header connectors are arranged on a standard 0.1inch (2.54mm) pitch. The horizontal pitch of the DIL Headers is 1.6 inches between the outer rows of the headers. The inner pins of the header form continuous power strips allowing a range of modules to be used together in one header subject to sufficient pins being available. The right hand side header has an inner column of 3.3V pins. The LHS header has an inner column of DGND (0V).

USB



The USB interface on the Drigmorn 4 is achieved using an FT2232H USB 2.0 High Speed (480Mb/s) to UART/FIFO device which can operate as a USB to dual serial / parallel ports with a variety of configurations.

The datasheet and drivers for this device are available from http://www.ftdichip.com. When appropriate drivers are installed the Drigmorn4 USB port should be detected as a serial port. Alternative data optimised drivers are also available from FTDI.

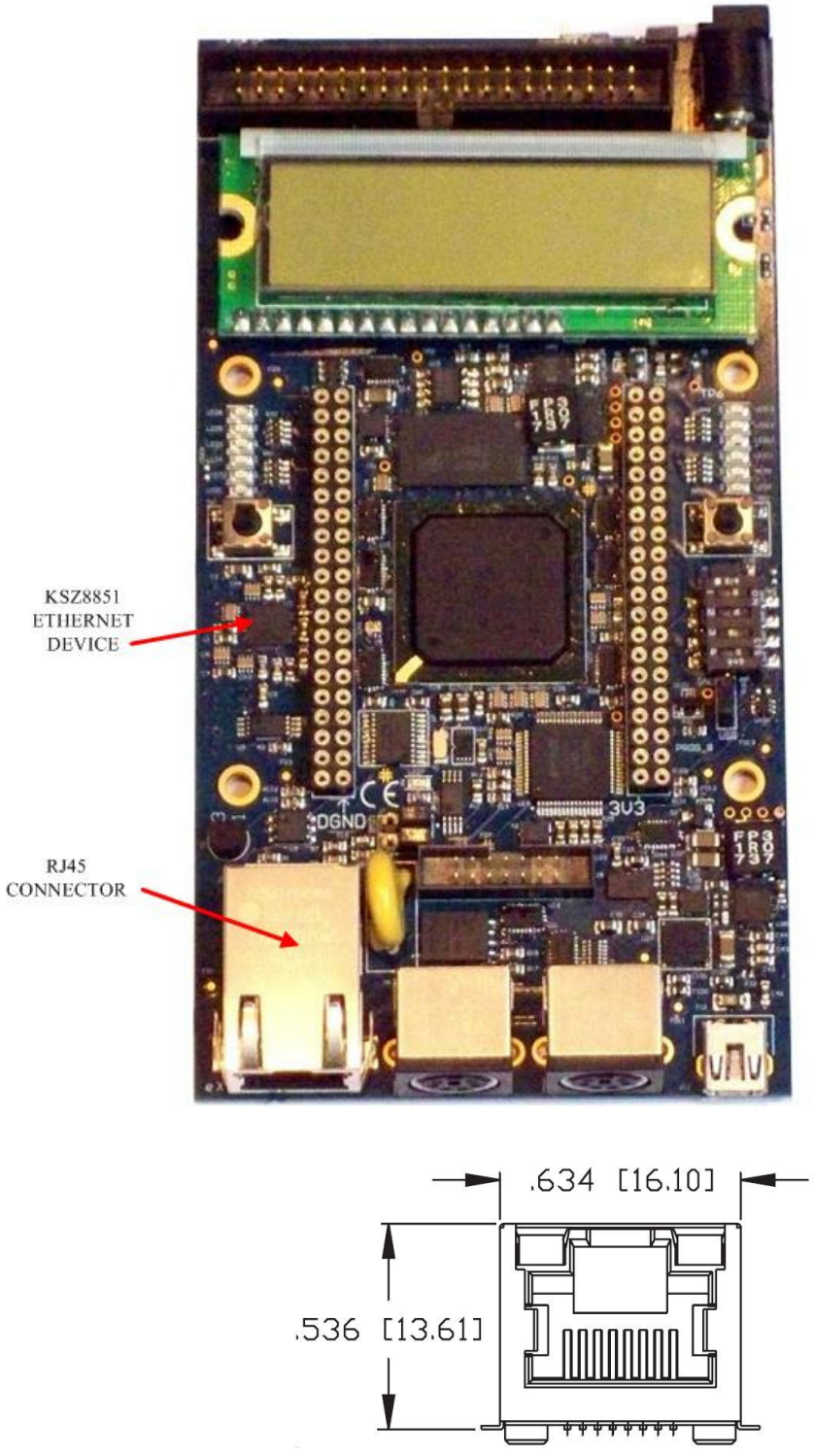
The FT2232H is connected to the Spartan-6 and has the capability of being configured in a variety of industry standard serial or parallel interfaces. It is supported by an AT93C46E 1Kbit serial EEPROM which is used for configuration data.

The FT2232H device is also connected into the JTAG chain for the FPGA so that reconfiguration of the FPGA over USB is possible. Jumper J14 will need to be set to the right position (between pins 2 and 3) for this to be possible.

The connections between the USB device and the FPGA are shown below:

SIGNAL	FT2232H PIN	FPGA PIN
ADBUS0	16	M7
ADBUS1	17	N7
ADBUS2	18	N1
ADBUS3	19	N4
ADBUS4	21	N3
ADBUS5	22	P7
ADBUS6	23	P6
ADBUS7	24	P4
ACBUS0	26	P5
ACBUS1	27	R1
ACBUS2	28	R3
ACBUS3	29	R4
ACBUS4	30	T1
ACBUS5	32	T2
ACBUS6	33	T4
ACBUS7	34	U1
BDBUS0	38	TCK
BDBUS1	39	TDI
BDBUS2	40	TDO
BDBUS3	41	TMS
BDBUS4	43	P3
BDBUS5	44	P2
BDBUS6	45	P1
BDBUS7	46	P8
BCBUS0	48	N6
BCBUS1	52	M2
BCBUS2	53	M5
BCBUS3	54	M6
BCBUS4	55	M8
BCBUS5	57	L3
BCBUS6	58	L1
BCBUS7	59	L6
#PWREN	60	K4
#SUSPEND	36	T3

ETHERNET



Drigmorn4 Ethernet connector showing dimensions

The Drigmorn4 Ethernet interface uses a Micrel KSZ8851SNL device. The KSZ8851 incorporates a Fast Ethernet MAC/PHY with an 8/16/32 bit generic host processor interface and SPI interface. All datasheets and support documentation can be found on Micrel's website www.micrel.com.

The connections between the KSZ8851 and the FPGA are as shown below:

KSZ8851 SIGNAL	KSZ8851 PIN	FPGA PIN	DRIGMORN4 SIGNAL
PME	2	D5	ETH_PME
INTRN	3	D3	ETH_INT_N
SI	31	D1	ETH_SD_IN
SO	27	C1	ETH_SD_OUT
CSN	26	H8	CSN_ETH
SCLK	28	C3	ETH_SCLK
RSTN	19	D2	RST_N_ETH
X1	20	E5	CLOCK_ETHERNET

Pin X1 of the KSZ8851SNL has been routed to the FPGA so that the Ethernet Clock frequency (25MHz) can be provided by the FPGA. You will need to implement this in any designs for the Ethernet to work.

The KSZ8851 has been provided with an AT93C46E EEPROM as required by the specification. It communicates to the 'outside world' via an RJ45 connector (Pulse J3006G21D) which has green and yellow LEDs which indicate whether a connection to an Ethernet hub is present.

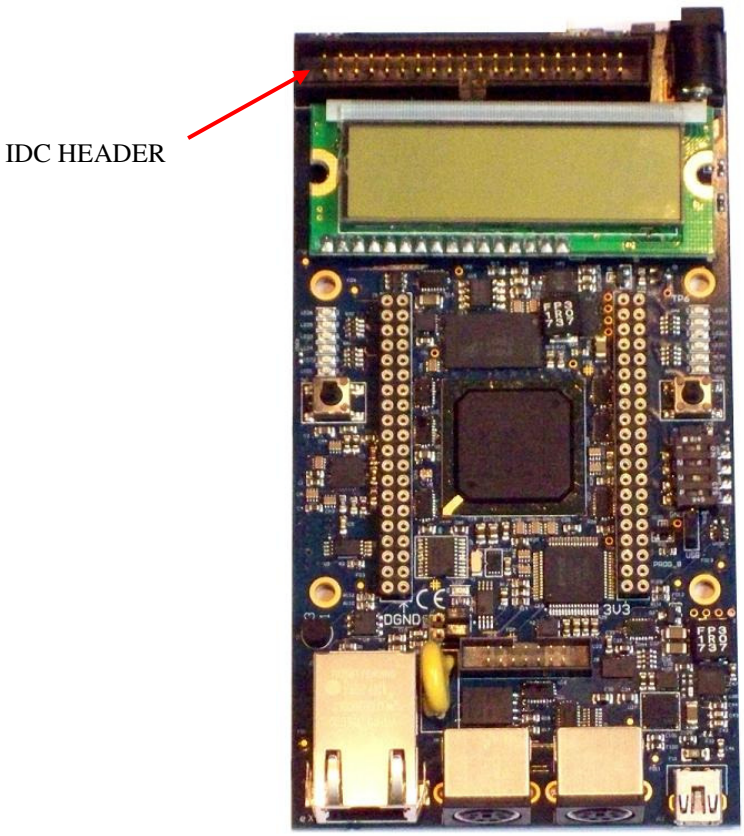
MAC ADDRESS DEVICES

The Drigmorn4 has two MAC address devices fitted which assign the boards unique identity numbers. The device used is a MAXIM DS2502-E48+, of which further details can be found on http://ww.maxim-ic.com. There are two sites on the Drigmorn4 for DS2502-E48+ devices, one is a 6 pin TSOC6 site, the other is a 3 pin TO-92 site. The 6 pin device is defined as Mac Address 1 and the 3 pin device is defined as Mac Address 2. It should be straightforward to determine which of these 2 devices is fitted on your board. The connections to the FPGA are shown below:

The table below shows the location of the MAC address devices on the Drigmorn 4.

MAC ADDRESS DEVICE	FPGA PIN
6 PIN TSOC6 DEVICE (MAC ADDRESS 1)	H3
3 PIN TO-92 DEVICE (MAC ADDRESS 2)	E6

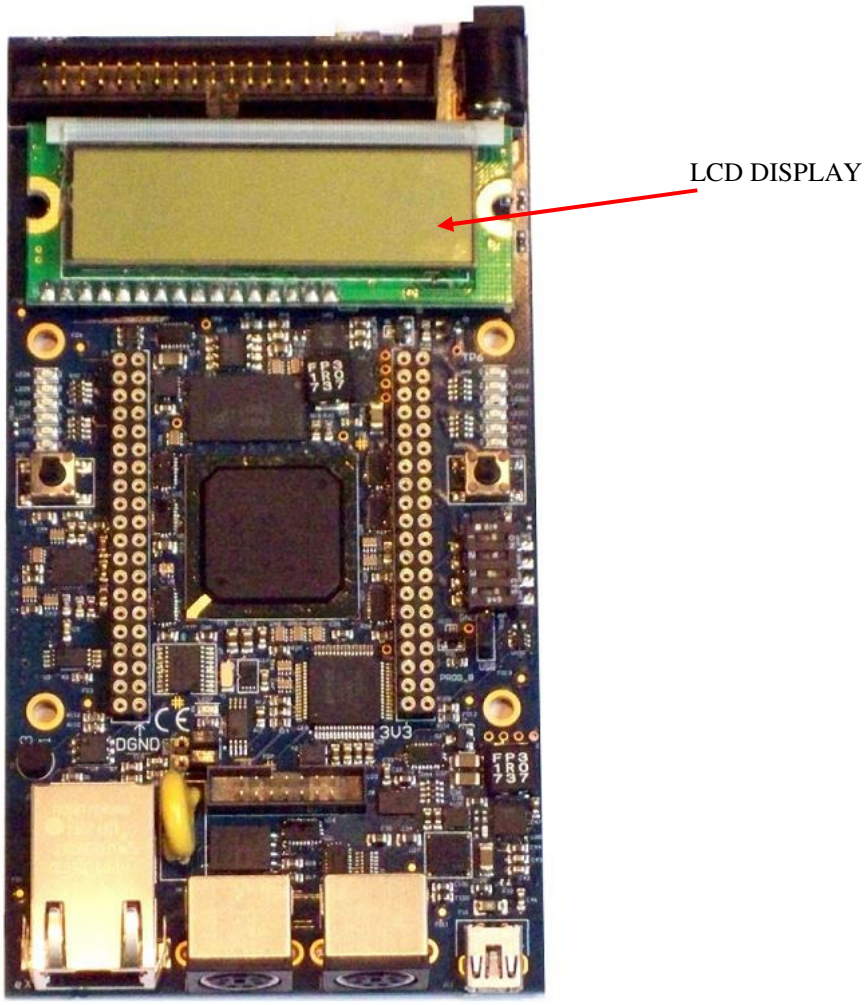
TOP IDC HEADER



At the top of the Drigmorn4 there is a 40 way IDC connector. This has 20 IO connections to the FPGA and 20 DGND(0V) connections. The IOs are wired directly to the Spartan-6 FPGA so signal voltage to these pins should not exceed 3.3V.The connections between the IDC connector and the FPGA are shown below. Pin 1 of the IDC header is defined as the pin on the left of the lower row of pins, as viewed from the front of the board. The odd numbered pins occupy the lower row of connections on the IDC header.

IDC PIN	SIGNAL NAME	FPGA PIN	IDC PIN	SIGNAL NAME	FPGA PIN
1	IDC_1	C5	21	IDC_11	D10
3	IDC_2	A5	23	IDC_12	C10
5	IDC_3	D6	25	IDC_13	Y15
7	IDC_4	C6	27	IDC_14	AB15
9	IDC_5	Y9	29	IDC_15	AA14
11	IDC_6	AB9	31	IDC_16	AB14
13	IDC_7	D9	33	IDC_17	Y13
15	IDC_8	C8	35	IDC_18	AB13
17	IDC_9	C9	37	IDC_19	W12
19	IDC_10	A9	39	IDC_20	Y12

LCD DISPLAY



The standard Drigmorn 4 LCD display is an LCM-S01602DTR/M display, which is 16x2 alpha-numerical display with a Hitachi HD44780 compatible chipset. More information on this at http://www.lumex.com/specs/LCM-S01602DTR%20M.pdf.

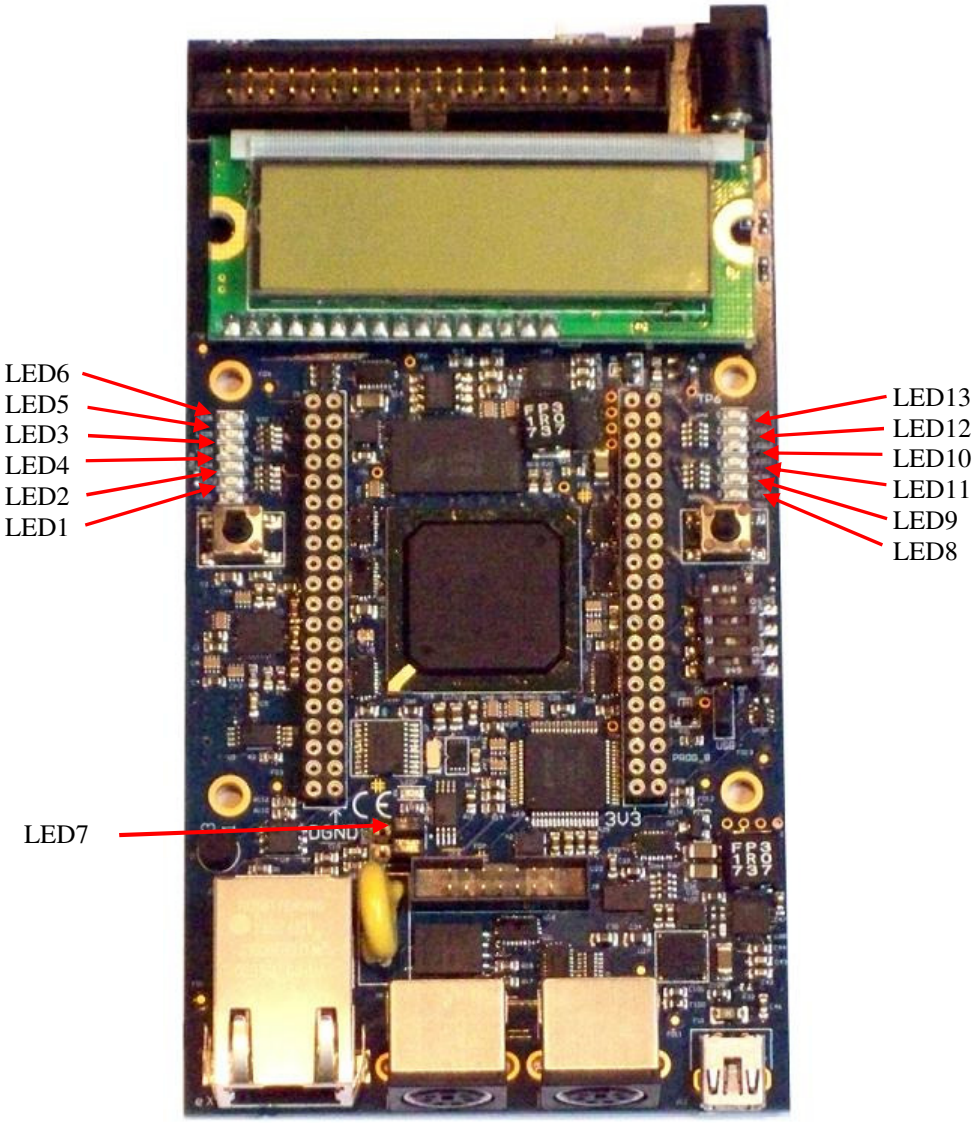
For OEM applications this LCD can be replaced by a 2x17 IDC header allowing remote location of the LCD or even reuse of the interface for other I/O functions. For these applications the 8 data signals are passed through bus switches giving 5V tolerance. The remaining signals of this interface are not protected for 5V operation and should only be used with voltages less than 3.3V.

For OEM applications we can offer other display solutions with graphic, colour LCD and OLED options. Contact us for specific requirements.

The IO pins used for the display are shown in the table below:

FUNCTION	FPGA PIN
Backlight ON	V11
RS	C14
R/W	C13
EN	D11
D0	C17
D1	A17
D2	D17
D3	E16
D4	A15
D5	C15
D6	D15
D7	D14

LEDS



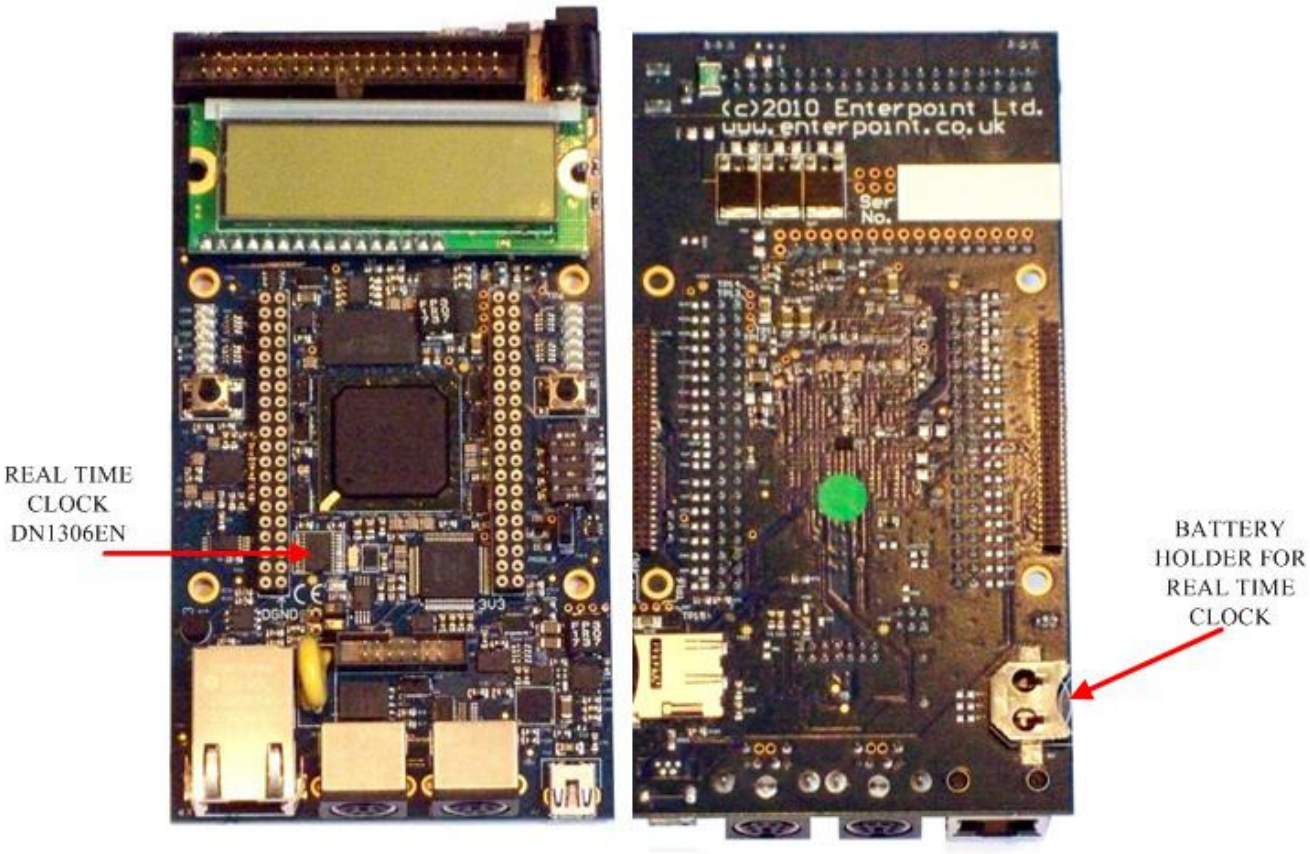
Drigmorn4 has 13 LEDs. There is a single red LED in the lower half of the board just below the Real Time Clock device, and 12 LEDs arranged into 4 blocks of three, one of each block being red, orange and green. This is to enable users to simulate a traffic light sequence. The LEDS may turn on dimly when power is applied to the unconfigured board. The relevant IO pin for an LED needs to be asserted low to ensure the specified LED turns on. The exception to this is LED7, for which the relevant IO pin should be asserted high.

Users may wish to visit out TechiTips section of the Enterpoint engineering website for tutorial and lab materials using Traffic Light LEDs. Our Techitips are located at http://www.enterpoint.co.uk/techitips/techitips.html.

The LEDS are connected to the FPGA as indicated below:

LED	FPGA PIN	COLOUR
1	A20	RED
2	A21	ORANGE
3	B22	GREEN
4	F16	GREEN
5	F17	ORANGE
6	C19	RED
7	K7	RED (SINGLE)
8	P17	RED
9	V20	ORANGE
10	U19	GREEN
11	W22	GREEN
12	W20	ORANGE
13	T20	RED

REAL TIME CLOCK



The Drigmorn4 has a Maxim DS1306EN+ Serial Alarm Real time clock device with a 32.768KHz crystal. Further information and datasheets for this device can be found on http://ww.maxim-ic.com.

The DS1306EN+ can provide a 32.768KHz clock, timed interrupts, and data storage features. Please consult the device datasheet for more details.

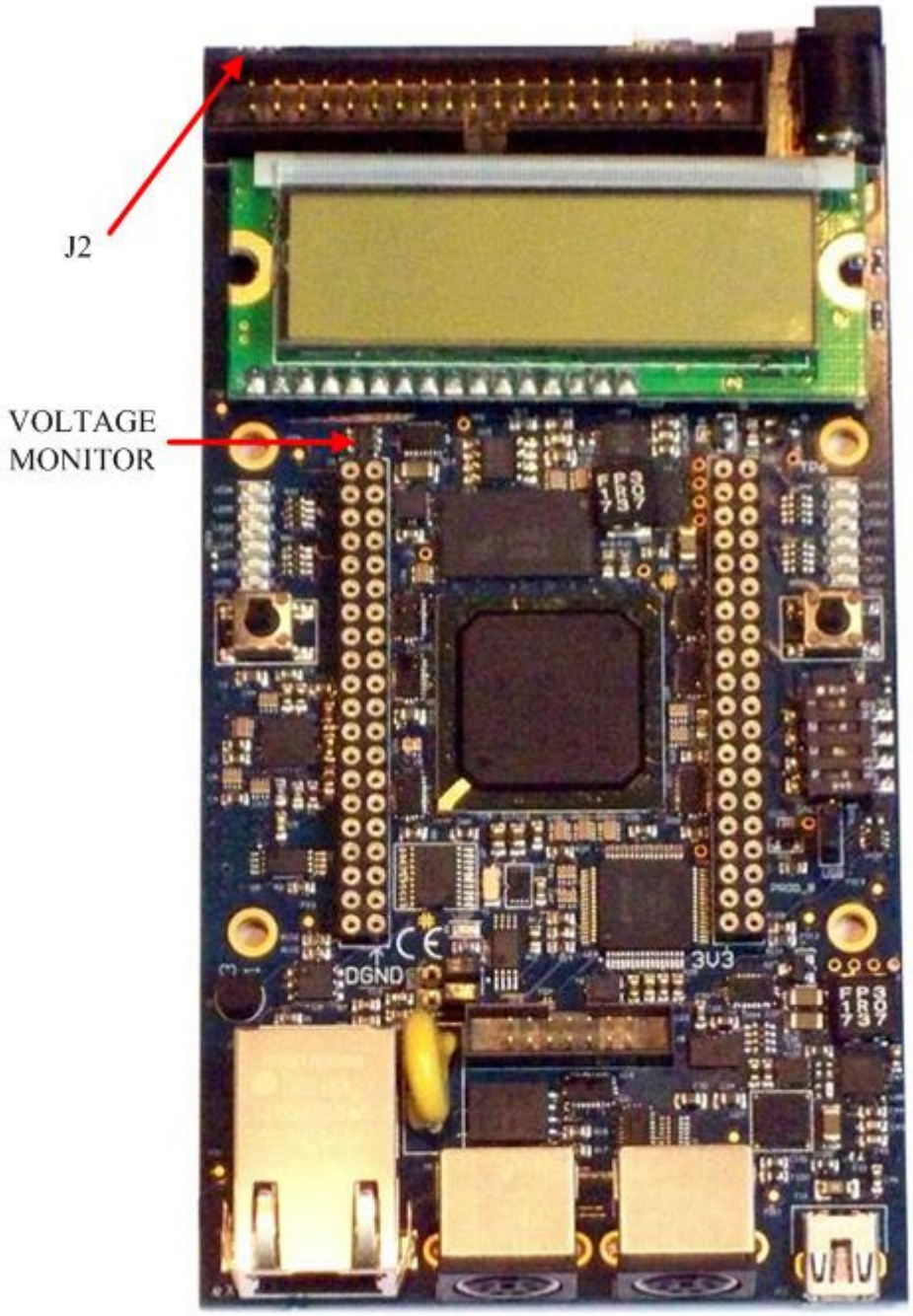
The DS1306EN+ is supported by a battery holder that can take CR1220/1225 battery types. We do not normally supply the battery to avoid shipping issues with batteries.

The connections between the Real Time Clock device and the FPGA are shown below:

SIGNAL	DS1306EN+ PIN	FPGA PIN
1HZ	9	F1
SDI	15	D1
INT1	8	F5
INT0#	7	F3
32KHZ	18	E1
SDO	16	E3
SCLK	14	C4
CE	12	B1

POWER MONITOR AND MASTER RESET

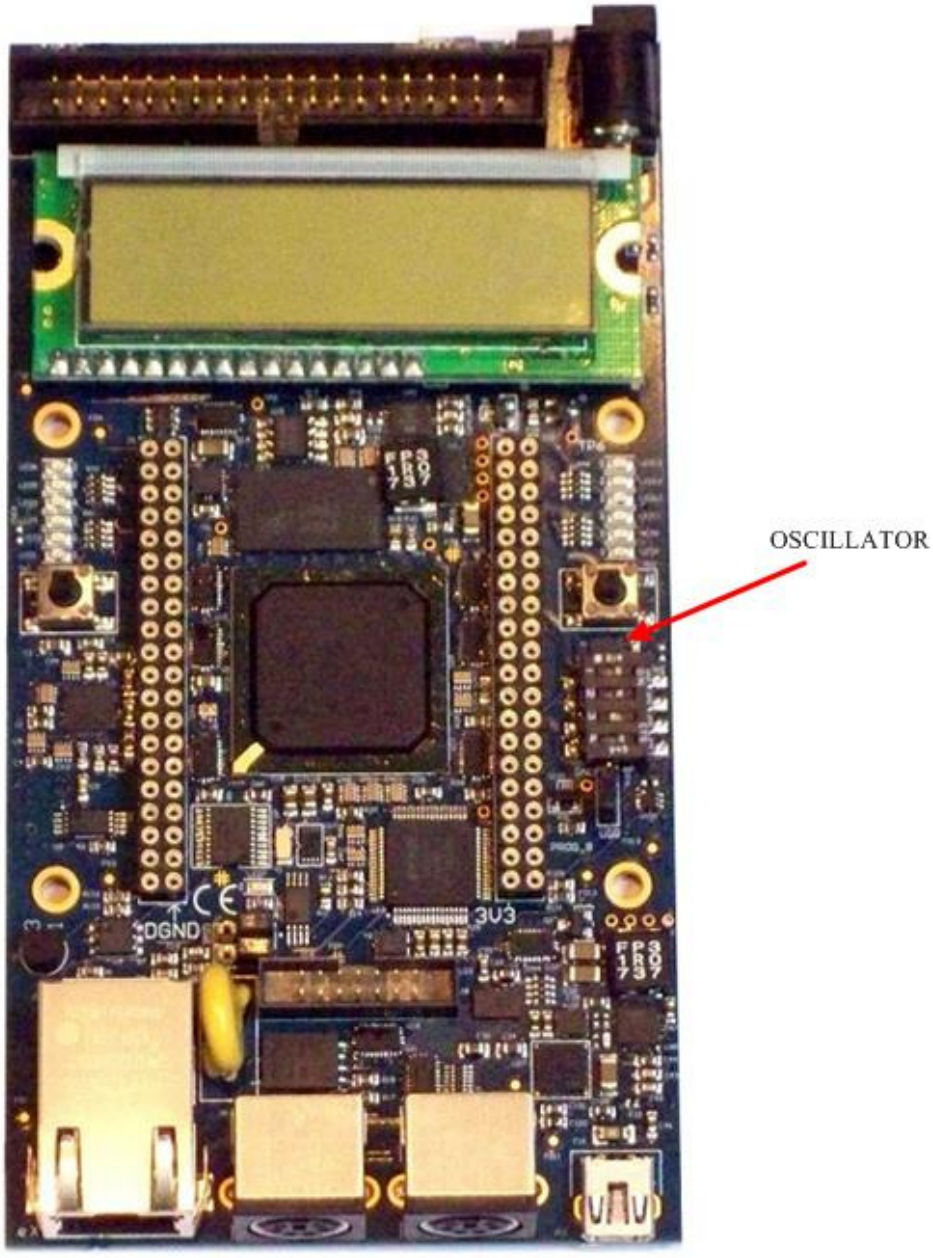
The Drigmorn4 has a voltage monitor which monitors the 3.3V, 1.2V and 0.75V supplies within the board. If any of these voltages are missing the reset signal is held active. Connector J2 (found at the very top left of the board) provides a manual reset facility. Placing a jumper between the centre pin of J2 and the leftmost pin (pin 1, 0V) will cause an active reset signal. This header can also be used for an external system reset with a remote switch or relay wired across the pins. The signal from the voltage monitor is connected to pin **C12** of the FPGA.



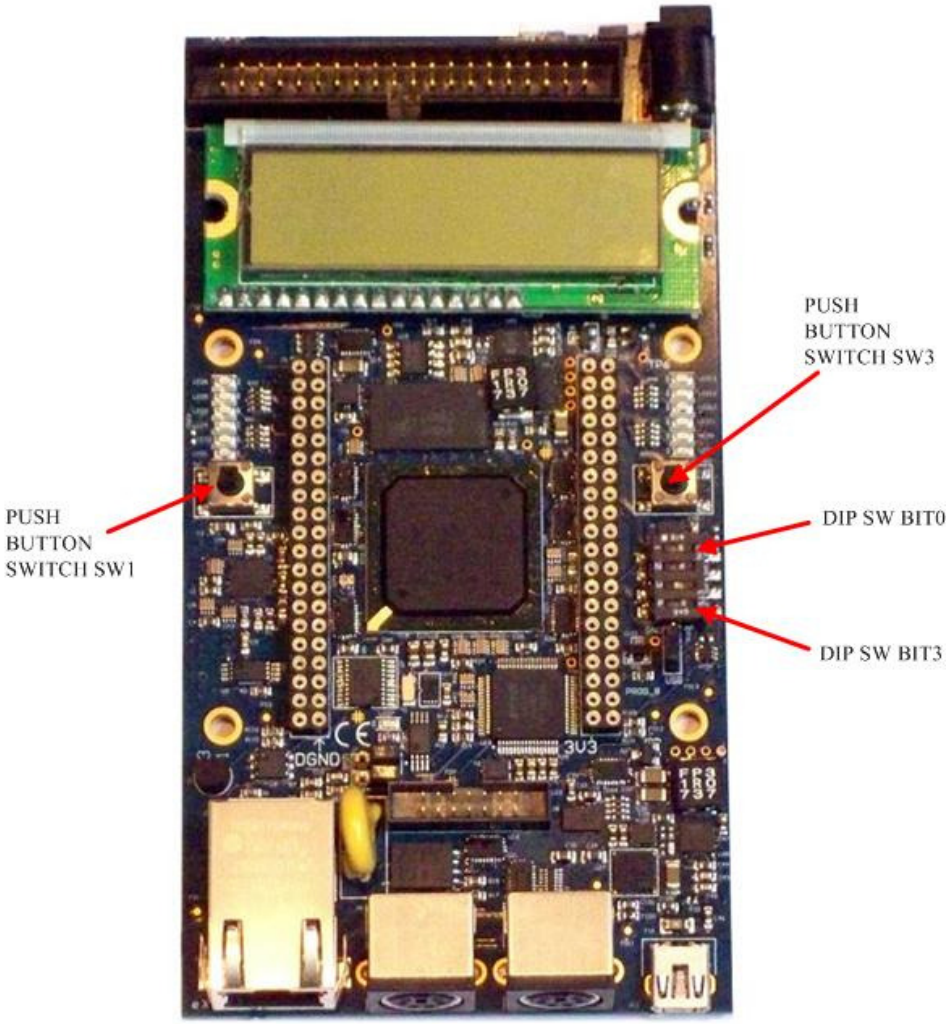
OSCILLATOR

The main oscillator on the Drigmorn4 is an ASEM 50MHz oscillator. The oscillator is situated as shown in and is connected to the FPGA on PIN AB11. The Drigmorn 4 also has a Clock Generator (see below) fitted with a 25MHz oscillator.

The Spartan-6 has PLLs and DCMs to produce multiples, divisions and phases of the clock for specific application requirements. Please consult the Spartan-6 datasheet available from the Xilinx website at http://www.xilinx.com if multiple clock signals are required.



SWITCHES



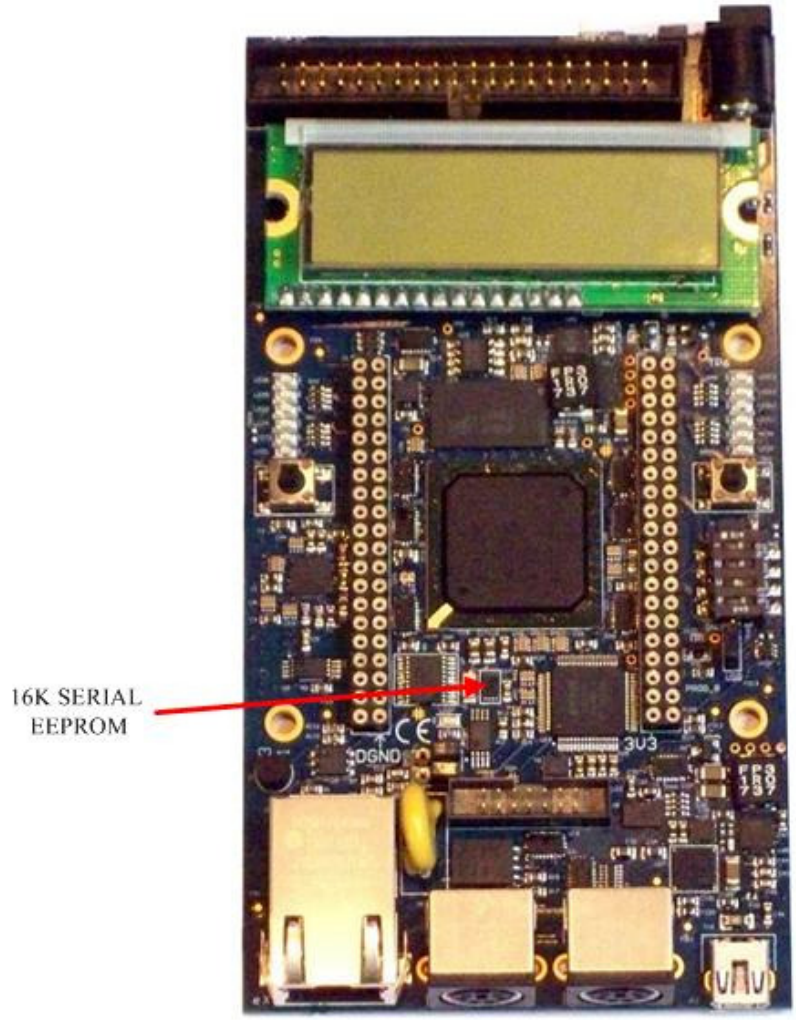
The Drigmorn4 has two push button switches and one 4 way DIP switch. To use these switches it is necessary to set the IO pins connected to the switches to have a pull up resistor in the FPGA. This is set in FPGA constraints file. Any switches pressed, or made, will then give a LOW signal at the FPGA otherwise a HIGH is seen. The two push button switches are connected to the following IO pins.

PB1 (RIGHT)	PB2 (LEFT)
Y4	F7

The four DIP switch bits are connected to the following IO pins.

BIT0	BIT1	BIT2	BIT3
M16	L15	M4	B3

16k SERIAL EEPROM



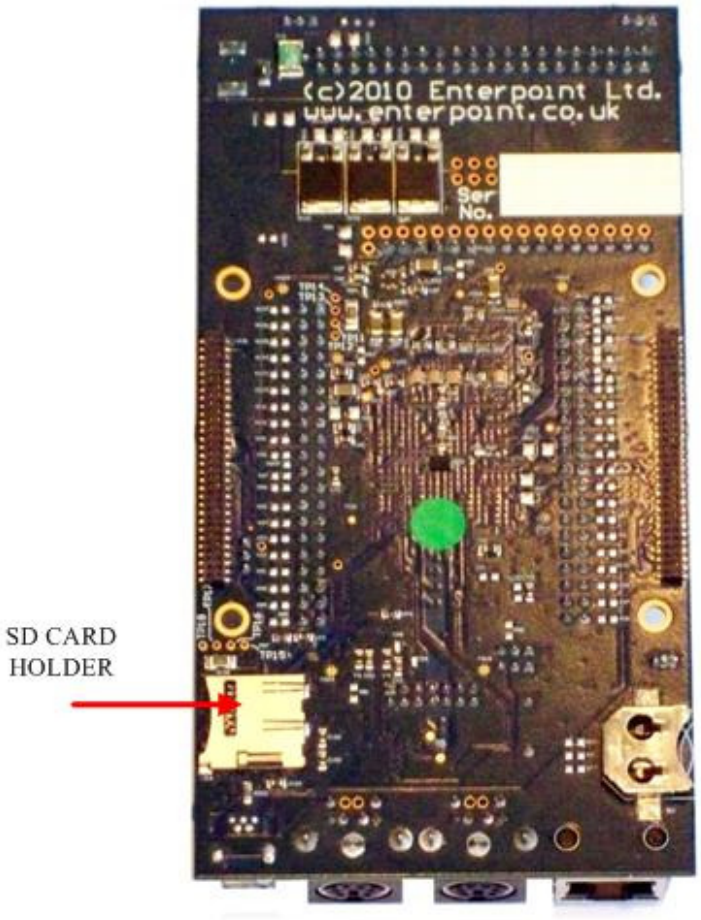
The Drigmorn4 has an Atmel AT24C16 EEPROM device, which use a simple Parallel address and single serial data line and clock. There is also a write protect line which can be used to electronically safeguard the information contained in the device.

This serial memory has 2048 words of 8 bits and employs a byte or page programming system. It can run at speeds up to 400 kHz. The EEPROM has the following connections to the FPGA:

EEPROM PIN	FPGA PIN
SDA	H1
SCL	H2
WP	G1

The address pins on this device are wired to DGND(0V).

MICRO SD CARD HOLDER



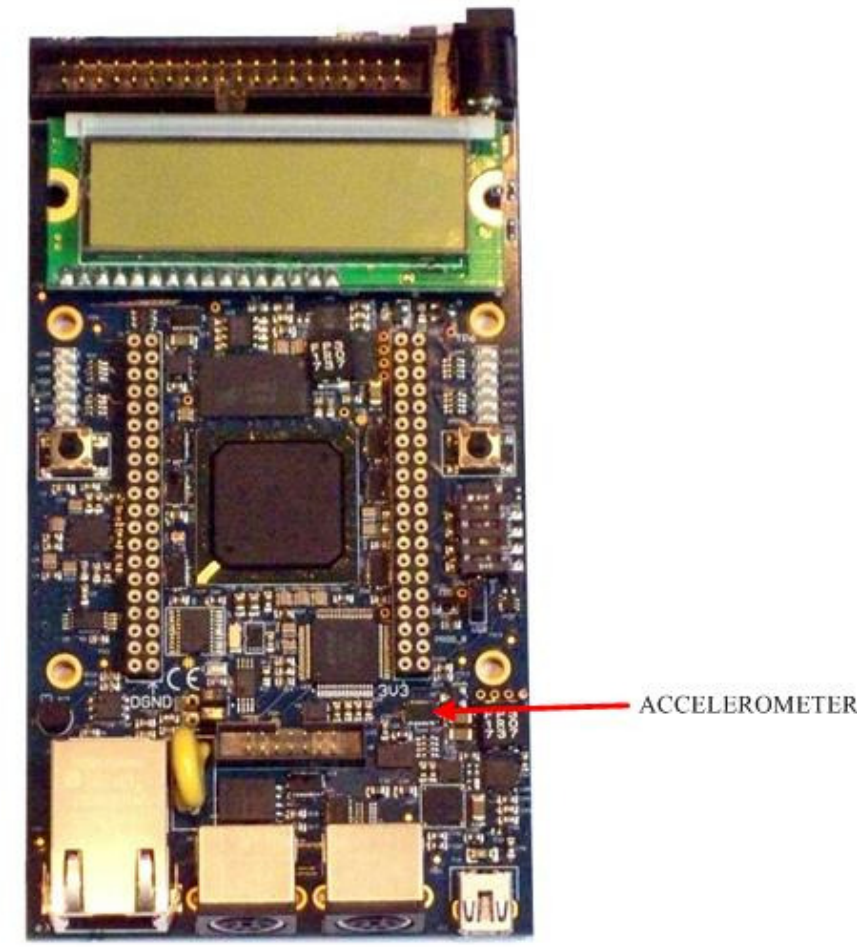
Further access to data can be achieved using the Micro SD Card Socket which is situated on the back of the Drigmorn 4 board. To use this socket in a design you may need to obtain a license from the SD Association at http://www.sdcard.org/home/.

The connections between the Micro SD Card Socket and the FPGA are shown below:

SDCARD SOCKET	FPGA PIN
DATA 0	Y2
DATA 1	W3
DATA 2	V1
DATA 3	V2
CMD	W1
CLK	V3
POWER_ON_N	M1

The POWER_ON_N pin must be set LOW for power to be supplied to the SDCARD Reader.

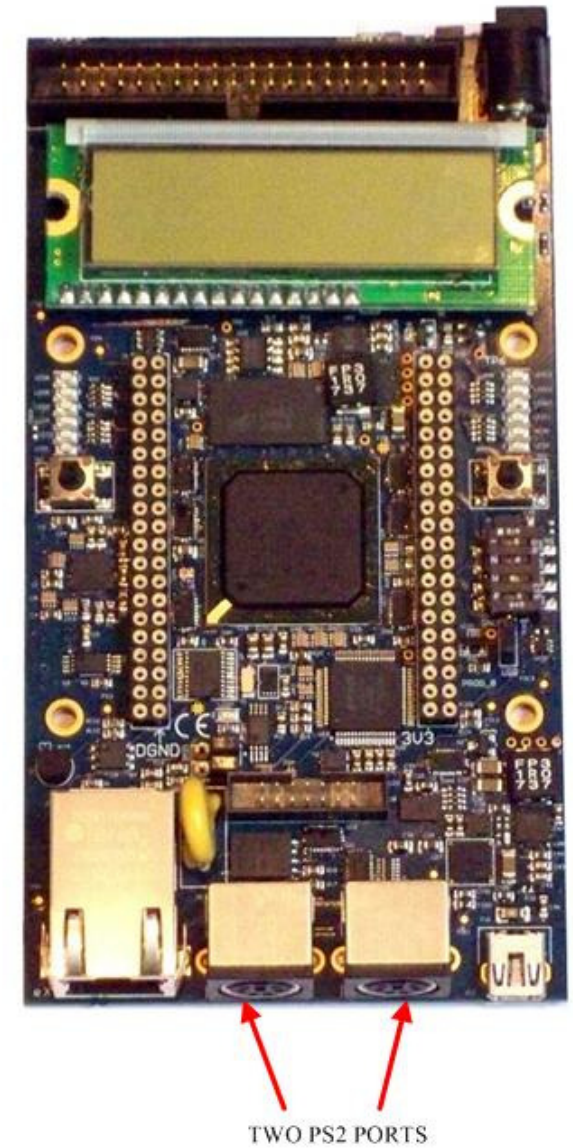
ACCELEROMETER

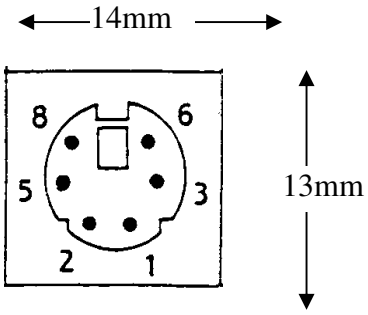


The Drigmorn 4 has an MMA7455L 3 axis accelerometer which has 3 sensitivity ranges: ±2g, ±4g and ±8g. Typical applications for this device are tilt and motion sensing, freefall detection and shock and vibration detection and these types of devices are used in cell phones, anti-theft equipment, pedometers, e-compasses and for 3d gaming. The datasheet for this accelerometer can be obtained from www.freescale.com. This device has both SPI and I2C interfaces. The connections between the accelerometer and the FPGA are shown below:

SIGNAL	ACC PIN	FPGA PIN
CS	7	J1
INT1/DRDY	8	J6
INT2	9	J7
SDO	12	K1
SDA/SDI/SDO	13	K2
SLC/SPC	14	K6
IADDR0	4	FIXED 0V

PS2



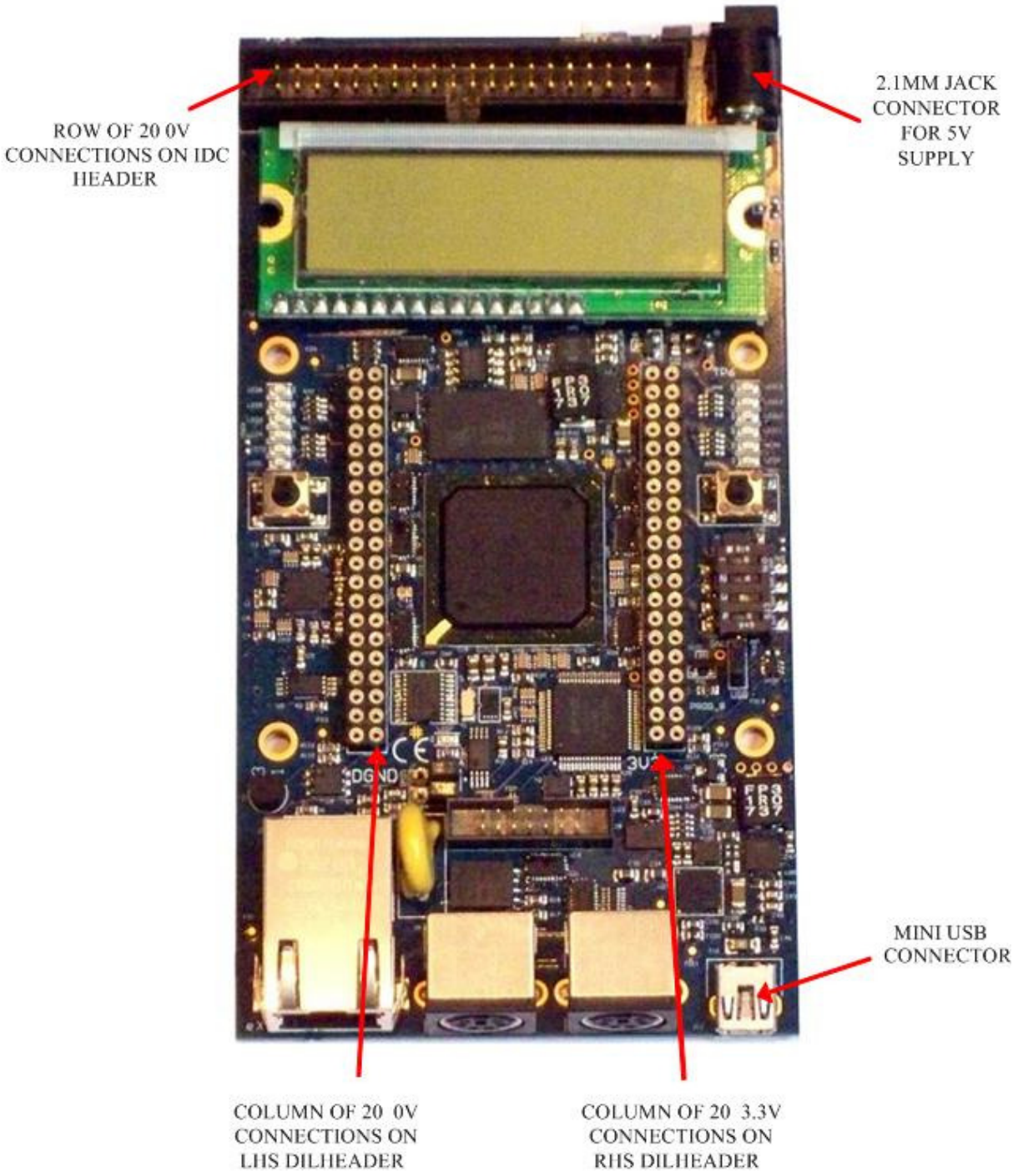


The Drigmorn4 has two PS2 ports which connect to the FPGA through bus switches and hence are 5V tolerant. These can be used to connect to a keyboard and mouse or for other user-defined functions.

The connections to the FPGA are shown below. Connector 1 is defined as the connector on the left.

PS2	FPGA PIN
CONNECTOR1 PIN 1 (LEFT)	G4
CONNECTOR1 PIN 2	G3
CONNECTOR1 PIN 3	Wired to 0V
CONNECTOR1 PIN 5	Wired to 5V
CONNECTOR1 PIN 6	G7
CONNECTOR1 PIN 8	F2
CONNECTOR2 PIN 1 (RIGHT)	H5
CONNECTOR2 PIN 2	H4
CONNECTOR2 PIN 3	Wired to 0V
CONNECTOR2 PIN 5	Wired to 5V
CONNECTOR2 PIN 6	H6
CONNECTOR2 PIN 8	G6

POWER CONNECTIONS

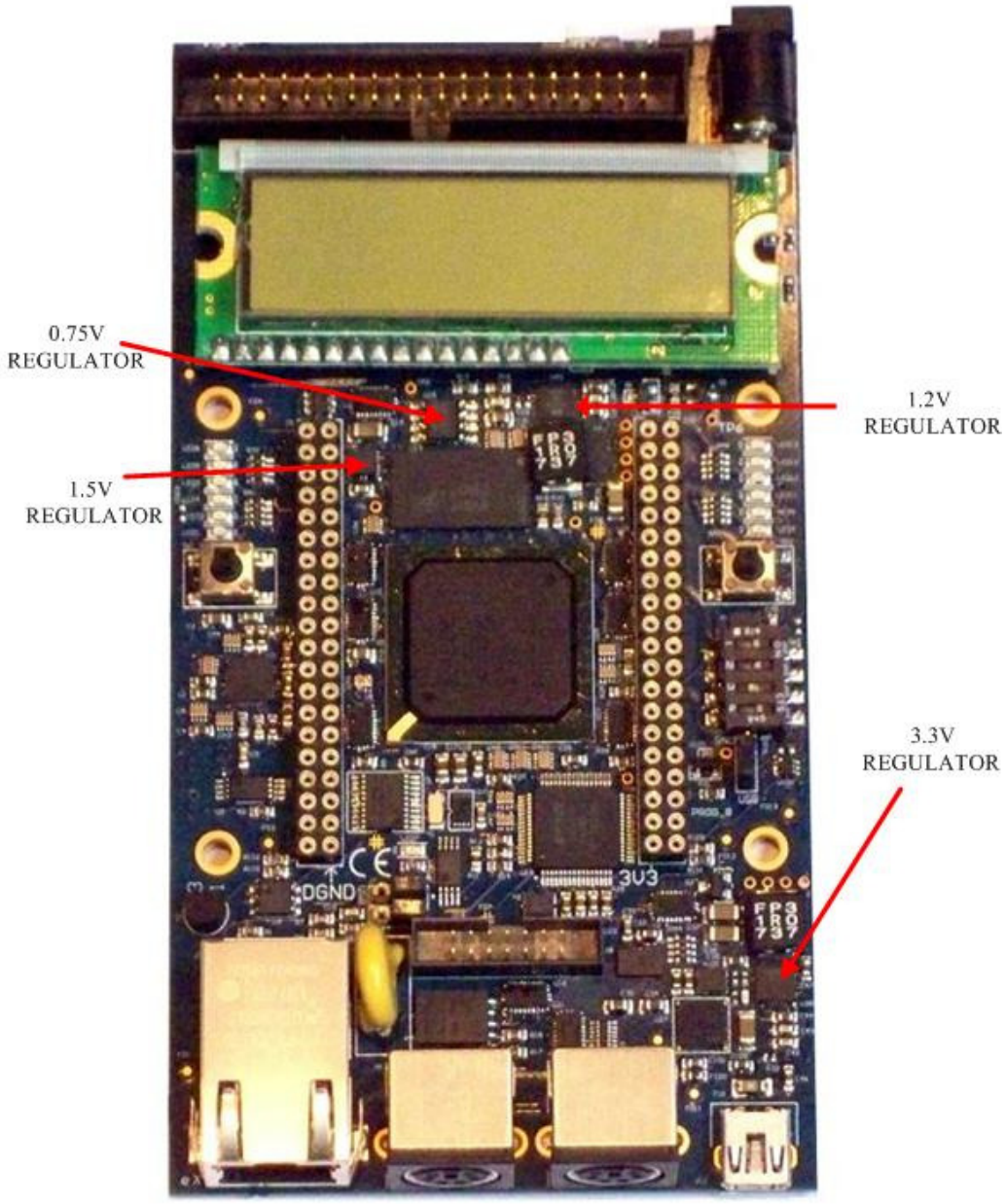

ROW OF 20 0V CONNECTIONS ON IDC HEADER
2.1MM JACK CONNECTOR FOR 5V SUPPLY
MINI USB CONNECTOR
COLUMN OF 20 0V CONNECTIONS ON LHS DILHEADER
COLUMN OF 20 3.3V CONNECTIONS ON RHS DILHEADER

Drigmorn4 is powered principally from the 2.1mm Jack socket. A limited supply can be provided using the USB connector, but since the current available from a USB port can be as low as 100mA this should be avoided unless you know that your design does not consume more current than this. A powered USB hub or a USB power supply can also be used. **Whatever power supply is used care should be taken not to exceed 5.5V input as this can cause damage to the Drigmorn4**. The

power from the jack connector is limited by a 2.6A resettable fuse, and the power from the USB connector is limited by a 1.1A resettable fuse.

0V and 3.3V are available on the DIL headers to power add-on modules or the user's hardware. The maximum current available from the 3.3v regulator is 6 amps, however the actual maximum current available will be limited by the fuse on the 5v supply

POWER REGULATORS



Drigmorn4 has four regulators supplying 3.3V, 1.5V, 1.2V and 0.75V power rails.

WARNING – REGULATORS CAN BECOME HOT IN NORMAL OPERATION ALONG WITH THE BOARDS THERMAL RELIEF. PLEASE DO NOT TOUCH OR PLACE HIGHLY FLAMABLE MATERIALS NEAR THESE DEVICES WHILST THE DRIGMORN4 BOARD IS IN OPERATION.

A Micrel MIC22600 regulator supplies 3.3V with a maximum current available of 6A. This powers the FPGA general I/O, DIL Header and other devices such the Ethernet controller and Real Time Clock.

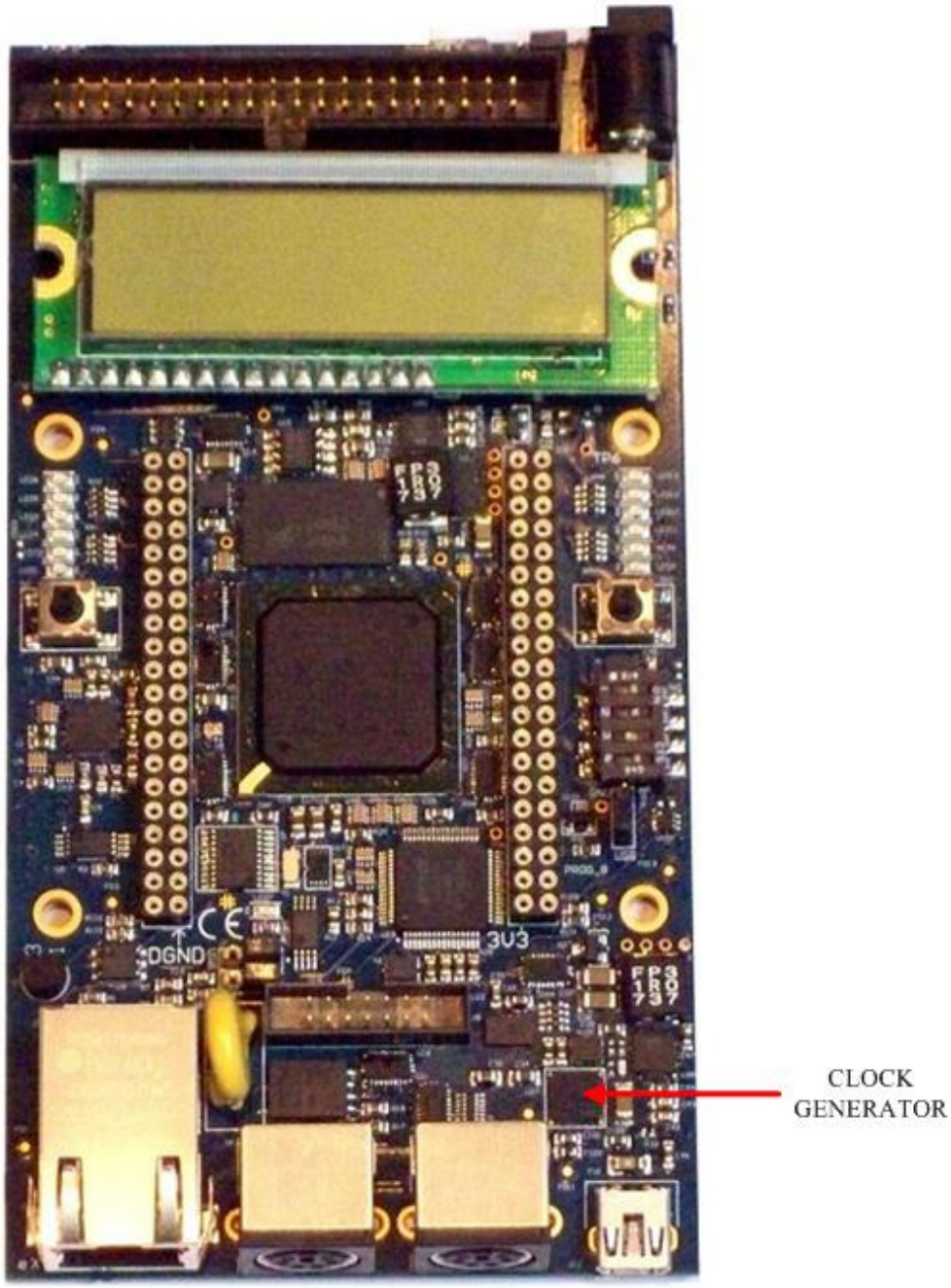
A Micrel MIC22600 regulator supplies 1.2V with a maximum current available of 6A. This is used for the core voltage of the FPGA .

An Empirion EP5388QI regulator supplies 1.5V with a maximum current of 600mA for the DDR3 and related FPGA I/O.

A National Semiconductor LP2996 push-pull regulator produces up to 1.5A at 0.75V. This supply is used as reference and termination voltage for the DDR3 memory and related FPGA I/O.

There is a small Standby Switch near the Jack socket which disables the voltage regulators. A small residual current into the board may be seen when the switch is in the ‘off’ position and the 5V supply to the board will still be active.

CLOCK GENERATOR



Drigmorn4 has an IDT5V19EE901NLGI clock generator capable of generating four single ended clocks and one differential clock which are all connected to FPGA. It can be used to generate clock frequencies in the range 4.9KHz to 500MHz. The clock generator is controlled by an I2C serial interface and has an internal EEPROM for storage of configuration data. Information and configuration software for this device are available from www.idt.com.

The connections between the Clock Generator and the FPGA are shown below:

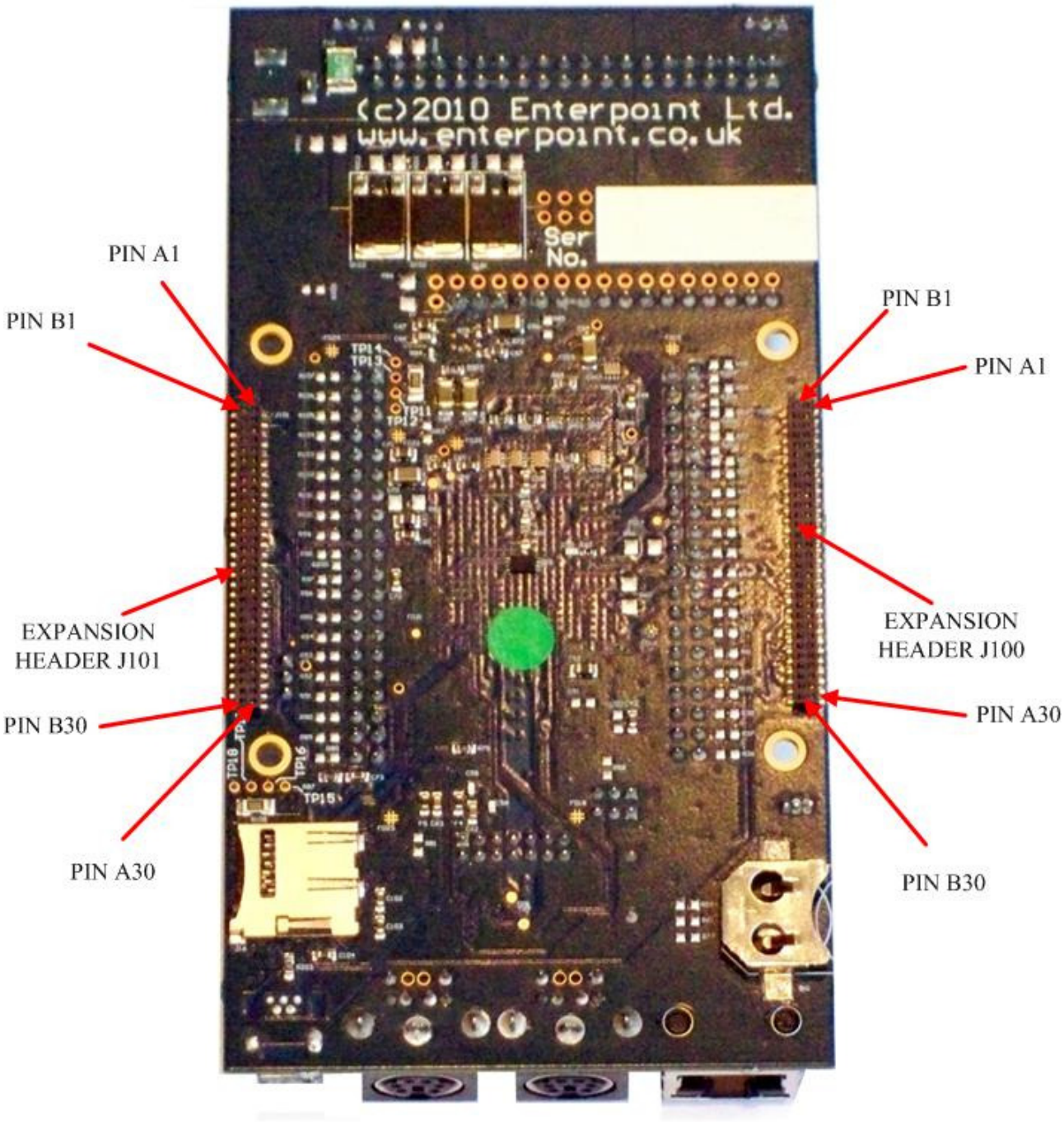
IDT5V19EE901 Function	IDT5V19EE901 Pin	FPGA Pin
CLK C	24	K5
P-CLK (Differential Clock –ve)	11	J4
P+ CLK (Differential Clock +ve)	10	K3
CLKB	8	M3
CLKA	7	L4
SDAT	18	W4
SCLK	19	U4
SEL2/SUSPEND	26	AB3
SHUTDOWN/OE	29	U3
CLK_X	30	J3

Signals shown in yellow are routed via a 4 bit multiplexer which enables these signals, if required, to be controlled from the USB device. In order for this to happen the signal on BCBUS4 must be asserted low, or a jumper should be fitted to J7(default). The legend on the PCB shows the positions for the jumper, marked FPGA if the FPGA is to control the clock generator (right side of J7) or USB if the control is from the FT2232H device (left side of J7).

When USB control is selected the signals will be routed as follows:

CLOCK GENERATOR SIGNAL	FT2232 PIN	USB SIGNAL
SHUTDOWN/OE	48	BCBUS0
SEL2/SUSPEND	52	BCBUS1
SCLK	53	BCBUS2
SDAT	54	BCBUS3

EXPANSION HEADERS



On the reverse side of Drigmorn4 are two CLP-130-02-L-D-A connectors which provide access to up to 38 LVDS pairs/76 single ended IO on the FPGA. These connections are not available for all FPGA sizes but they are all connected for the XC6SLX150 device. The connections between these expansion headers and the FPGA are shown below. The suffix of the IO function denotes the FPGA Bank into which it connects.

J100 PIN	SIGNAL NAME	FPGA PIN	FUNCTION	J100 PIN	SIGNAL NAME	FPGA PIN	FUNCTION
A1	DGND			B1	EXP_P14	V19	IO_L9P_2
A2	EXP_P35	T18	IO_L4P_2	B2	EXP_N14	V18	IO_L9N_2
A3	EXP_N35	T17	IO_L4N_2	B3	EXP_P16	T16	IO_L7P_2
A4	DGND			B4	EXP_N16	T15	IO_L7N_2
A5	DGND			B5	EXP_P13	R16	IO_L10P_2
A6	EXP_P7	E14	IO_L47P_0	B6	EXP_N13	R15	IO_L10N_2
A7	EXP_N7	F15	IO_L47N_0	B7	EXP_P6	F14	IO_L48P_0
A8	DGND			B8	EXP_N6	H14	IO_L48N_0
A9	DGND			B9	EXP_P8	H13	IO_L46P_0
A10	EXP_P10	H12	IO_L44P_0	B10	EXP_N8	G13	IO_L46N_0
A11	EXP_N10	F12	IO_L44N_0	B11	EXP_P11	E12	IO_L43P_0
A12	DGND			B12	EXP_N11	D12	IO_L43N_0
A13	DGND			B13	EXP_P1	G11	IO_L18P_0
A14	EXP_P2	E10	IO_L17P_0	B14	EXP_N1	H11	IO_L18N_0
A15	EXP_N2	F10	IO_L17N_0	B15	EXP_P3	G9	IO_L16P_0
A16	DGND			B16	EXP_N3	H10	IO_L16N_0
A17	DGND			B17	EXP_P9	F13	IO_L45P_0
A18	EXP_CLOCK1_P		(NOTE C)	B18	EXP_N9	D13	IO_L45N_0
A19	EXP_CLOCK1_N		(NOTE C)	B19	EXP_P4	G8	IO_L15P_0
A20	EXP_SUSPEND		N15 (NOTE A)	B20	EXP_N4	F9	IO_L15N_0
A21	EXP_SCP		(NOTE B)	B21	EXP_P33		
A22	PB1		Y4	B22	EXP_N33		
A23	PB2		F7	B23	EXP_P5	E8	IO_L14P_0
A24	REG1_EN		(NOTE D)	B24	EXP_N5	F8	IO_L14N_0
A25	REG2_EN		(NOTE D)	B25	EXP_P30	T8	IO_L51P_2
A26	DGND			B26	EXP_N30	U8	IO_L51N_2
A27	DGND			B27	EXP_P31	U9	IO_L50P_2
A28	DGND			B28	EXP_N31	V9	IO_L50N_2
A29	DGND			B29	EXP_P36	W6	IO_L53P_2
A30	DGND			B30	EXP_N36	Y6	IO_L53N_2

	AVAILABLE ON LX150 , LX100
	AVAILABLE ON LX150, LX100, LX75, LX25
	AVAILABLE ON LX150, LX100, LX25
	AVAILABLE ON LX150, LX100, LX75, LX45
	AVAILABLE ON LX150, LX100, LX45, LX25
	AVAILABLE ON LX150, LX100, LX45
	AVAILABLE ON LX150, LX45, LX25
	AVAILABLE ON LX150, LX45
	AVAILABLE ON ALL DEVICES

J101 PIN	SIGNAL NAME	FPGA PIN	FUNCTION	J101 PIN	SIGNAL NAME	FPGA PIN	FUNCTION
A1	EXP_P12	V17	IO_L11P_2	B1	DGND		
A2	EXP_N12	W17	IO_L11N_2	B2	EXP_P17	W18	IO_L6P_2
A3	EXP_P15	U17	IO_L8P_2	B3	EXP_N17	Y18	IO_L6N_2
A4	EXP_N15	U16	IO_L8N_2	B4	DGND		
A5	EXP_P19	Y16	IO_L17P_2	B5	DGND		
A6	EXP_N19	W15	IO_L17N_2	B6	EXP_P21	T14	IO_L23P_2
A7	EXP_P20	W14	IO_L20P_2	B7	EXP_N21	R13	IO_L23N_2
A8	EXP_N20	Y14	IO_L20N_2	B8	DGND		
A9	EXP_P18	V13	IO_L18P_2	B9	DGND		
A10	EXP_N18	W13	IO_L18N_2	B10	EXP_P38	U14	IO_L14P_2
A11	EXP_P32	T7	IO_L60P_2	B11	EXP_N38	U13	IO_L14N_2
A12	EXP_N32	R7	IO_L60N_2	B12	EXP_CLK_SEL 1		(NOTE C)
A13	EXP_P22	T12	IO_L22P_2	B13	EXP_CLK_SEL 0		(NOTE C)
A14	EXP_N22	U12	IO_L22N_2	B14	EXP_P37	AA10	IO_L41P_2
A15	EXP_P23	R11	IO_L40P_2	B15	EXP_N37	AB10	IO_L41N_2
A16	EXP_N23	T11	IO_L40N_2	B16	EXP_CLOCK_SRC_SEL		(NOTE C)
A17	EXP_P24	W10	IO_L44P_2	B17	EXP_CLOCK		(NOTE C)
A18	EXP_N24	Y10	IO_L44N_2	B18	5V		(NOTE E)
A19	EXP_P25	W9	IO_L47P_2	B19	5V		(NOTE E)
A20	EXP_N25	Y9	IO_L47N_2	B20	5V		(NOTE E)
A21	EXP_P26	W8	IO_L46P_2	B21	5V		(NOTE E)
A22	EXP_N26	V7	IO_L46N_2	B22	V5		(NOTE E)
A23	EXP_P27	Y5	IO_L54P_2	B23	5V_FEED_1		(NOTE E)
A24	EXP_N27	AB5	IO_L54N_2	B24	5V_FEED_1		(NOTE E)
A25	EXP_P28	Y7	IO_L48P_2	B25	5V_FEED_1		(NOTE E)
A26	EXP_N28	AB7	IO_L48N_2	B26	5V_FEED_1		(NOTE E)
A27	EXP_P29	T10	IO_L52P_2	B27	5V_FEED_2		(NOTE E)
A28	EXP_N29	U10	IO_L52N_2	B28	5V_FEED_2		(NOTE E)
A29	EXP_P34	U6	IO_L63P_2	B29	5V_FEED_2		(NOTE E)
A30	EXP_N34	V5	IO_L63N_2	B30	5V_FEED_2		(NOTE E)

	AVAILABLE ON LX150, LX100, LX45, LX25
	AVAILABLE ON LX150, LX100, LX45
	AVAILABLE ON LX150, LX45, LX25
	AVAILABLE ON LX150, LX45
	AVAILABLE ON ALL DEVICES

NOTES

A. This pin is connected to the main suspend pin of the Spartan6 and is intended for use where the FPGA needs to be shut down from an external device e.g. for power saving. Leaving this pin unconnected allows the FPGA to function

normally. Asserting the pin HIGH (3v3) will shut the FPGA down. There is a 100ohm resistor connected between this pin and DGND.

B. EXP_SCP connects to 4 resistor sites (R204 to R207) which connect to the top 4 Left hand side DIL Header pins. This is to allow an external device connected to J100 to connect with a user's module plugged into the DIL Headers. Drigmorn4 boards are normally shipped with these resistors not fitted. If customer requires any of these resistors to be fitted it is advised that they specify which are required so that they can be fitted before the board is shipped. Enterpoint Ltd cannot be responsible for damage to the Drigmorn4 board by poor soldering.

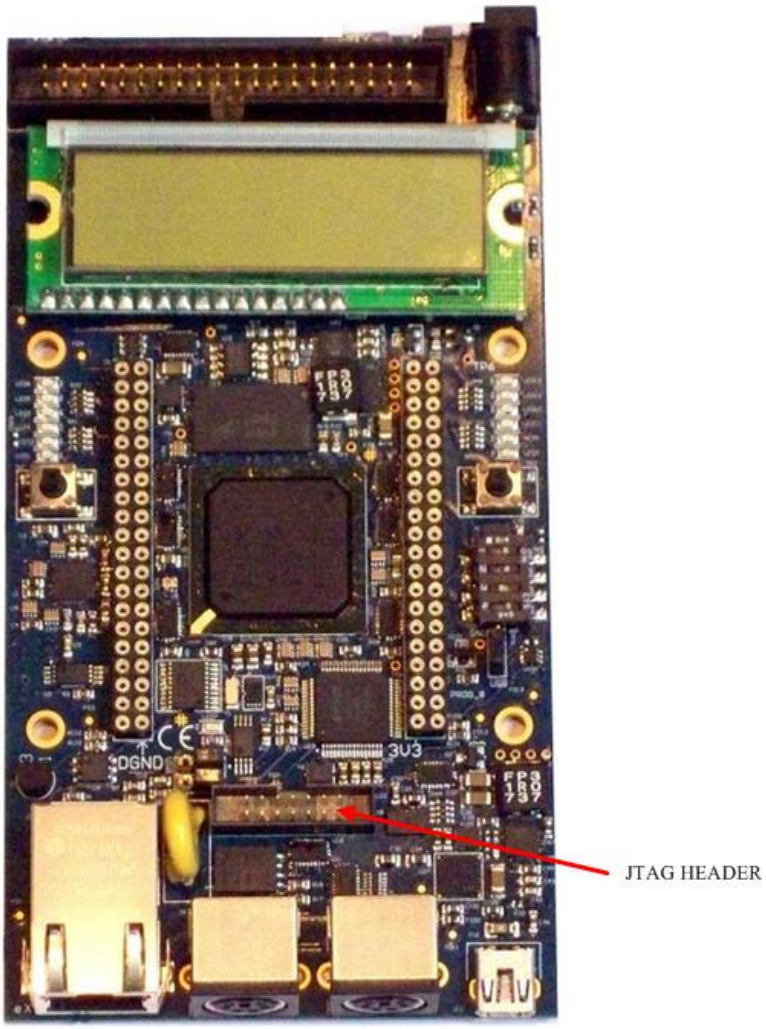
C. There are 6 connections between the expansion headers and the Clock Generator. This is to allow an external device connected to the expansion headers to provide an alternative clock source to the 25MHz oscillator provided on Drigmorn4, to select the clock source and to access clock signals from the Clock Generator. The connections between the Expansion headers and the Clock Generator are shown below:

SIGNAL NAME	EXPANSION HEADER PIN	CLOCK GENERATOR PIN
EXP_CLOCK	B17	5
EXP_CLOCK_SRC_SEL	B16	20
EXP_CLOCK_SEL0	B13	28
EXP_CLOCK_SEL1	B12	27
EXP_CLK1_P	A18	14
EXP_CLK1_N	A19	15

D. There are two signals on the expansion header which allow the main regulators on the DN4 to be shut down for purposes of power saving. REG1_EN controls the 1.2V regulator and REG2_EN controls the 3.3V regulator. These signals should be asserted LOW to shut down a regulator, leaving them unconnected allows the regulators to function normally.

E. There is a choice of power sources for the expansion header 5v supply. The supply on pins 18-22 of J101 is either from the Jack socket on Drigmorn4 (J13) or from the USB connection to Drigmorn4 depending upon the setting of jumper J11. Pins B23 to B26 could, if required, be used to supply 5v from the expansion headers to power the Drigmorn4. Pins B27 to B30 could be used for a second alternative power supply e.g. a solar panel or a battery. **The Supply voltage should not exceed 5.5V as this would cause irreparable damage to the Voltage Regulators on Drigmorn4.**

Programming Drigmorn4



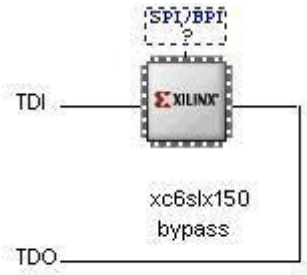
The programming of the FPGA and SPI Flash parts on Drigmorn4 is achieved using the JTAG interface. Principally it is anticipated that a JTAG connection will be used in conjunction with Xilinx ISE software although other alternatives do exist including self re-programming. The Spartan-6 series needs to be programmed using ISE 11 or higher. Versions of ISE prior to 11 do not support Spartan-6. The full version of the Xilinx tools is required to program the XC6SLX150-2FGG484C. The free Webpack version of ISE is sufficient to support the smaller versions of the FPGA.

There is a single JTAG chain on Drigmorn4. The JTAG chain allows the programming of the Spartan-6 and SPI Flash device.

The JTAG connector has a layout as follows (top view):

GND	GND	GND	GND	GND	GND	GND
3V3	TMS	TCK	TDO	TDI	NC	NC

Using iMPACT Boundary Scan the JTAG chain appears like this:



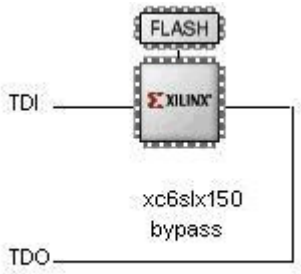
1. Programming the FPGA directly.

Direct JTAG programming of the Spartan-6 FPGA is volatile and the FPGA will lose its configuration every time the board power is cycled. For sustained use of an FPGA design programming the design into the Flash memory is recommended (see 2 and 3 below).

Direct JTAG programming using .bit files is useful for fast, temporary programming during development of FPGA programs. Right click the icon representing the Spartan-6 FPGA and choose 'Assign New Configuration File'. Navigate to your .bit file and choose 'OPEN'. The next dialogue box will offer to add a flash memory and you should decline. Right click the icon representing the Spartan-6 FPGA and choose 'Program'. On the next dialogue box ensure that the 'Verify' box is not checked. (If it is you should uncheck it, failure to do this will result in error messages being displayed). Click OK. The Spartan-6 will program. This process is very quick (typically one second)

2. Programming the SPI flash memory using Boundary Scan.

Once the SPI Flash memory has been programmed, the Spartan-6 device will automatically load from the Flash memory at power up. Generation of suitable Flash memory files (.mcs) can be achieved using ISE iMPACT's Prom File Formatter. Right click on the icon representing the Spartan-6 and choose 'Add SPI/BPI Flash' Navigate to your programming file (.mcs) and click OPEN. Use the next dialogue box to select SPI flash and M25P128. Data width should be set to 1. The flash memory should appear as shown below.



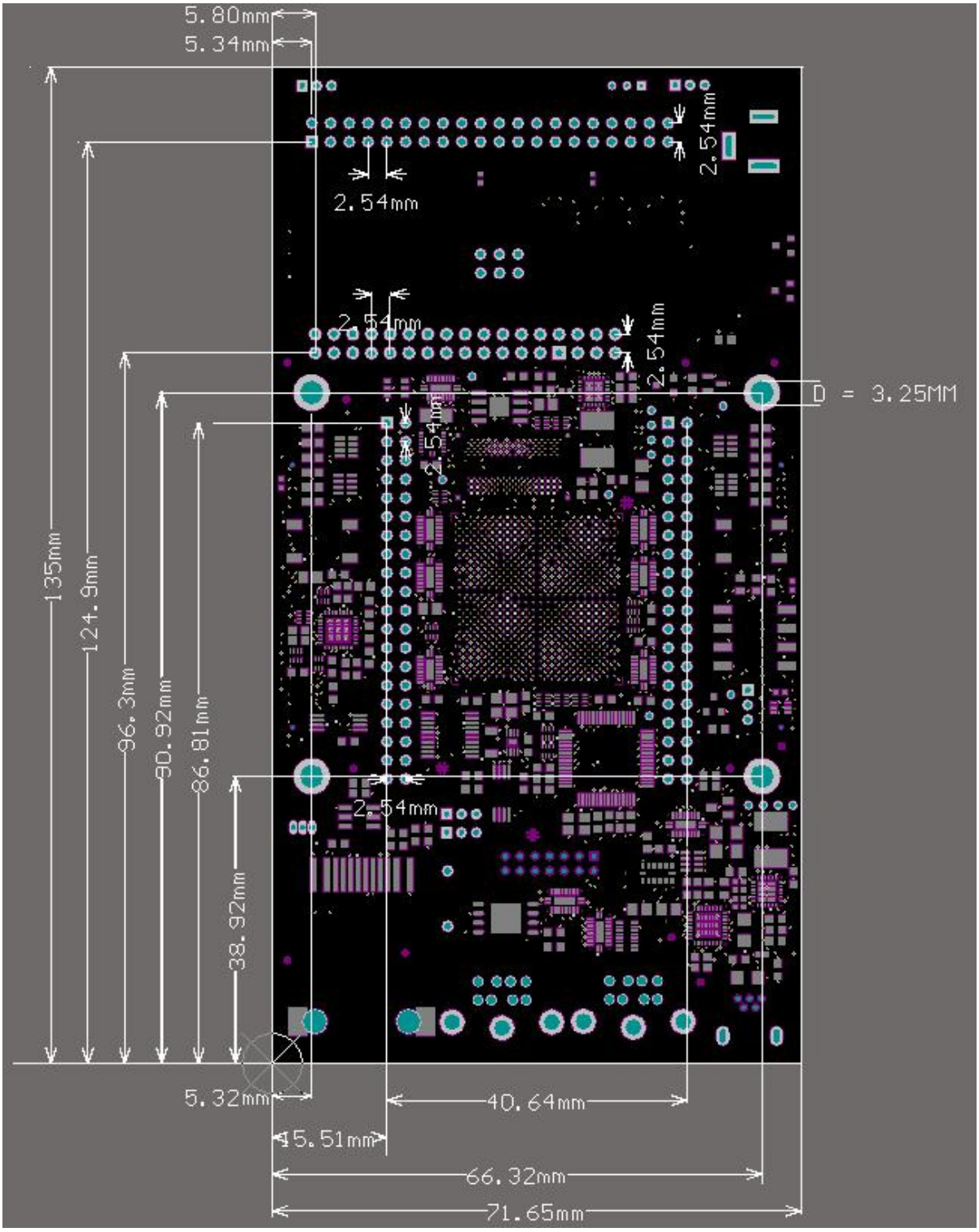
Right click on the icon representing the flash memory and choose ‘Program’ to load your program into the device. It is recommended that options to ‘Verify’ and ‘Erase before programming’ are chosen. Otherwise all defaults can be accepted. The programming operation will take some time (at least 3 or 4 minutes).

Depending upon the settings used when generating the bitfile using ISE, it will take up to 20 seconds for the XC6LX150 to configure upon power-up. In order to decrease this time the following process can be followed:

1. In the main ISE menu, right-click ‘Generate Programming file’. Choose Properties.
2. On the left hand side of the Process Properties Dialogue box, choose Configuration Options.
3. The first item on the menu which appears on the right hand side of the dialogue box is ‘Configuration Rate’. The default setting is 2. Increase this number. The maximum value we suggest is 22. Choose ‘Apply’ and ‘OK’.
4. Generate the program file as normal.

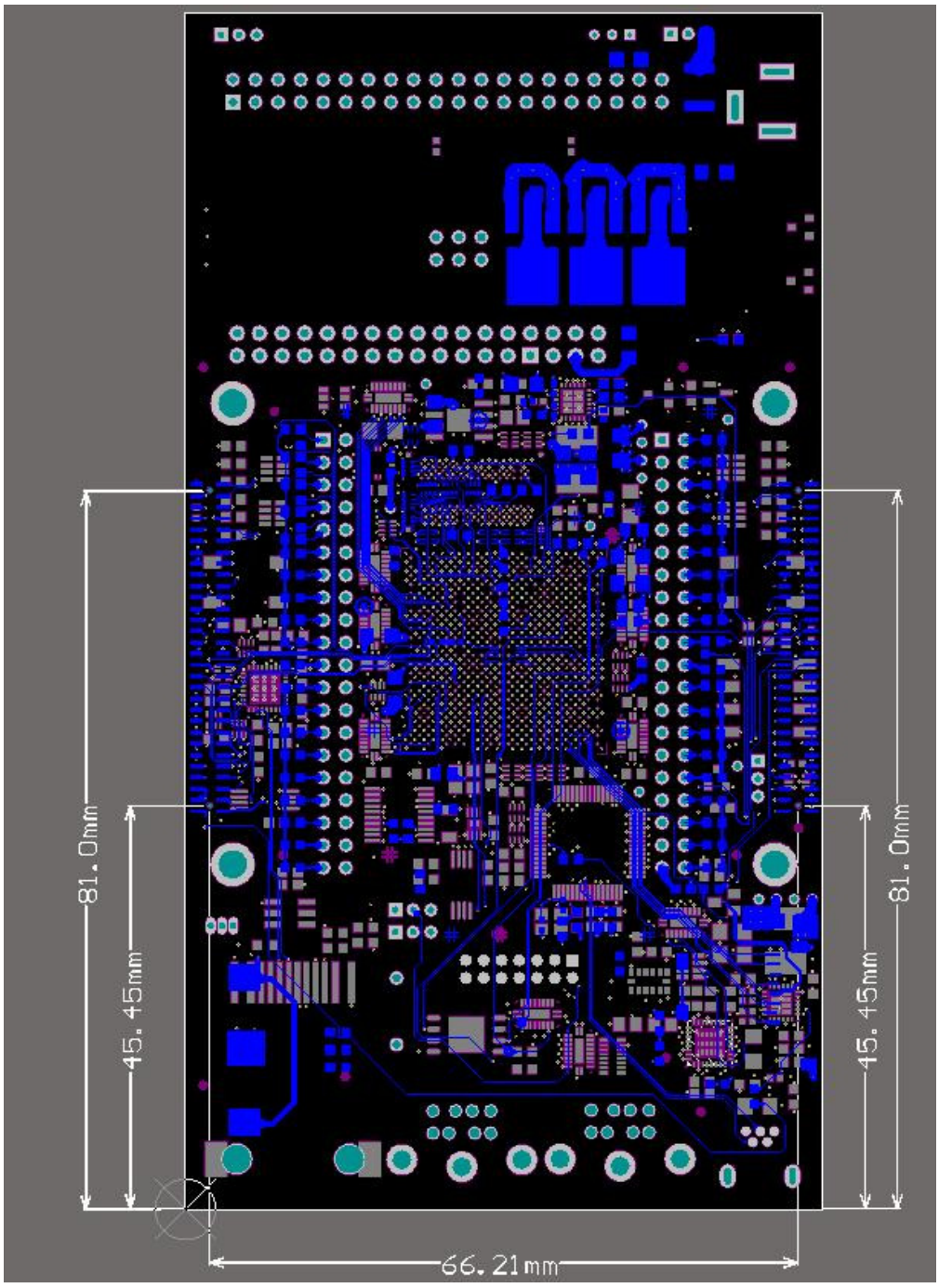
MECHANICAL ARRANGEMENT

The Dimensions on the drawings below are millimetres (mm). All sizes quoted are subject to manufacturing tolerances and should only be used as a general guide.



Locations of mounting holes and headers

The socket pins on the DIL headers are arranged on a 2.45mm (0.1inch) pitch



Location of Expansion headers (measured to holes for locating pegs)

The heights of the components, measured from the lower surface of the board are as follows:

Upper surface of LCD display: 12.5mm
Ethernet connector: 15.3mm
USB connector: 5.5mm
PS2 connectors: 14.7mm
Micro SD card holder, measured from top surface of PCB to bottom of SD card holder: 2.6mm
The PCB is 1.6mm thick

Medical and Safety Critical Use

Drigmorn4 boards are not authorised for the use in, or use in the design of, medical or other safety critical systems without the express written person of the Board of Enterpoint. If such use is allowed the said use will be entirely the responsibility of the user. Enterpoint Ltd will accepts no liability for any failure or defect of the Drigmorn4 board, or its design, when it is used in any medical or safety critical application.

Warranty

Drigmorn4 comes with a 90 day return to base warranty. Do not attempt to solder connections to the Drigmorn4. Enterpoint reserves the right not honour a warranty if the failure is due to soldering or other maltreatment of the Drigmorn4 board.

Outside warranty Enterpoint offers a fixed price repair or replacement service. We reserve the right not to offer this service where a Drigmorn4 has been maltreated or otherwise deliberately damaged. Please contact support if you need to use this service.

Other specialised warranty programs can be offered to users of multiple Enterpoint products. Please contact sales on boardsales@enterpoint.co.uk if you are interested in these types of warranty,

Support

Please check our FAQ page for this product first before contacting support. FAQ is located at http://www.enterpoint.co.uk/drigmorn/Drigmorn4_faq.html. Telephone and email support is offered during normal United Kingdom working hours (GMT or GMT + 1) 9.00am to 5.00pm.

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